Hewlett-Packard Company
hp AlphaServer ES45 68/1250

SPECint_rate2000 = 42.0
SPECint_rate_base2000 = 38.8

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Copies</th>
<th>Base Runtime</th>
<th>Base Ratio</th>
<th>Copies</th>
<th>Runtime</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>164.gzip</td>
<td>4</td>
<td>244</td>
<td>26.6</td>
<td>4</td>
<td>241</td>
<td>26.9</td>
</tr>
<tr>
<td>175.vpr</td>
<td>4</td>
<td>164</td>
<td>39.6</td>
<td>4</td>
<td>160</td>
<td>40.6</td>
</tr>
<tr>
<td>176.gcc</td>
<td>4</td>
<td>123</td>
<td>41.7</td>
<td>4</td>
<td>113</td>
<td>45.0</td>
</tr>
<tr>
<td>181.mcf</td>
<td>4</td>
<td>175</td>
<td>47.7</td>
<td>4</td>
<td>138</td>
<td>60.7</td>
</tr>
<tr>
<td>186.crafty</td>
<td>4</td>
<td>98.1</td>
<td>47.3</td>
<td>4</td>
<td>98.1</td>
<td>47.3</td>
</tr>
<tr>
<td>197.parser</td>
<td>4</td>
<td>309</td>
<td>27.0</td>
<td>4</td>
<td>255</td>
<td>32.7</td>
</tr>
<tr>
<td>252.eon</td>
<td>4</td>
<td>132</td>
<td>45.9</td>
<td>4</td>
<td>138</td>
<td>43.8</td>
</tr>
<tr>
<td>253.perlbmk</td>
<td>4</td>
<td>222</td>
<td>37.7</td>
<td>4</td>
<td>211</td>
<td>39.6</td>
</tr>
<tr>
<td>254.gap</td>
<td>4</td>
<td>219</td>
<td>23.4</td>
<td>4</td>
<td>179</td>
<td>28.5</td>
</tr>
<tr>
<td>255.vortex</td>
<td>4</td>
<td>164</td>
<td>53.7</td>
<td>4</td>
<td>146</td>
<td>60.3</td>
</tr>
<tr>
<td>256.bzip2</td>
<td>4</td>
<td>163</td>
<td>42.6</td>
<td>4</td>
<td>153</td>
<td>45.5</td>
</tr>
<tr>
<td>300.twolf</td>
<td>4</td>
<td>292</td>
<td>47.6</td>
<td>4</td>
<td>292</td>
<td>47.6</td>
</tr>
</tbody>
</table>

**Hardware**

CPU: Alpha 21264C
CPU MHz: 1250
FPU: Integrated
CPU(s) enabled: 4 cores, 4 chips, 1 core/chip
CPU(s) orderable: 1 to 4
Parallel: No
Primary Cache: 64KB(I)+64KB(D) on chip
Secondary Cache: 16MB off chip per CPU
L3 Cache: None
Other Cache: None
Memory: 16GB
Disk Subsystem: 9 GB SCSI
Other Hardware: None

**Software**

Operating System: Tru64 UNIX T5.1B
Compiler: Compaq C V6.5-011-48C5K
Spike V5.2 (506 48C5K)
Compaq C++ V6.5-028
File System: ufs
System State: Multi-user

**Notes/Tuning Information**

Baseline C : cc -arch ev6 -fast +CFB ONESTEP
C++: cxx -arch ev6 -O2 ONESTEP

Peak:
All but 252.eon: cc -q3 -arch ev6 ONESTEP
164.gzip: -fast -O4 -non_shared +CFB
175.vpr: -fast -O4 -assume restricted_pointers +CFB
176.gcc: -fast -O4 -xtaso_short -all -ldensemalloc -none +CFB +IFB
181.mcf: -fast -xtaso_short +CFB +IFB +PFB
186.crafty: same as base
197.parser: -fast -O4 -xtaso_short -non_shared +CFB
252.eon: cxx -arch ev6 -O2 -all -ldensemalloc -none
253.perlbmk: -fast -non_shared +CFB +IFB
254.gap: -fast -O4 -non_shared +CFB +IFB +PFB
255.vortex: -fast -non_shared +CFB +IFB
256.bzip2: -fast -O4 -non_shared +CFB
300.twolf: -fast -O4 -ldensemalloc -non_shared +CFB +IFB
**Notes/Tuning Information (Continued)**

Most benchmarks are built using one or more types of profile-driven feedback. The types used are designated by abbreviations in the notes:

+CFB: Code generation is optimized by the compiler, using feedback from a training run. These commands are done before the first compile (in phase "fdo_pre0"):

```
mkdir /tmp/pp
rm -f /tmp/pp/${baseexe}*
```

and these flags are added to the first and second compiles:

```
PASS1_CFLAGS = -prof_gen_noopt -prof_dir /tmp/pp
PASS2_CFLAGS = -prof_use -prof_dir /tmp/pp
```

(Peak builds use /tmp/pp above; base builds use /tmp/pb.)

+IFB: Icache usage is improved by the post-link-time optimizer Spike, using feedback from a training run. These commands are used (in phase "fdo_postN"):

```
mv ${baseexe} oldexe
spike oldexe -feedback oldexe -o ${baseexe}
```

+PFB: Prefetches are improved by the post-link-time optimizer Spike, using feedback from a training run. These commands are used (in phase "fdo_post_makeN"):

```
rm -f *Counts*
mv ${baseexe} oldexe
pixie -stats dstride oldexe 1>pixie.out 2>pixie.err
mv oldexe.pixie ${baseexe}
```

A training run is carried out (in phase "fdo_runN"), and then this command (in phase "fdo_postN"):

```
spike oldexe -fb oldexe -stride_prefetch -o ${baseexe}
```

When Spike is used for both Icache and Prefetch improvements, only one spike command is actually issued, with the Icache options followed by the Prefetch options.

**vm:**

```
vm_bigpg_enabled = 1
vm_bigpg_thresh=16
vm_swap_eager = 0
```

**proc:**

```
max_per_proc_address_space = 0x400000000000
max_per_proc_data_size = 0x400000000000
max_per_proc_stack_size = 0x400000000000
max_proc_per_user = 2048
max_threads_per_user = 0
maxusers = 16384
per_proc_address_space = 0x400000000000
```
Hewlett-Packard Company  
hp AlphaServer ES45 68/1250  

SPECint\_rate2000 = 42.0  
SPECint\_rate\_base2000 = 38.8

Notes/Tuning Information (Continued)
per\_proc\_data\_size = 0x400000000000  
per\_proc\_stack\_size = 0x400000000000

Portability:  
gcc:  -Dalloca=\_\_builtin\_alloca;  
     crafty:  -DALPHA  
perlbmk:  -DSPEC\_CPU2000\_DUNIX;  
vortex:  -DSPEC\_CPU2000\_LP64  
gap:  -DSYS\_HAS\_CALLOC\_PROTO  
     -DSYS\_IS\_BSD  -DSYS\_HAS\_IOCTL\_PROTO  
     -DSPEC\_CPU2000\_LP64