SPEC® CINT2006 Result

Hewlett-Packard Company

ProLiant BL460c
(1.86 GHz, Intel Xeon processor E5320)

SPECint®2006 = 11.9
SPECint_base2006 = 11.4

CPU2006 license: 3
Test sponsor: Hewlett-Packard Company
Tested by: Hewlett-Packard Company
Hardware Availability: Jan-2007
Software Availability: Nov-2006

Test date: Feb-2007

SPECint2006 = 11.9
SPECint_base2006 = 11.4

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECint2006</th>
<th>SPECint_base2006</th>
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</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>10.1</td>
<td>13.6</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>8.62</td>
<td>9.84</td>
</tr>
<tr>
<td>403.gcc</td>
<td>8.32</td>
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<tr>
<td>429.mcf</td>
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<tr>
<td>445.gobmk</td>
<td>8.04</td>
<td>12.3</td>
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<tr>
<td>464.h264ref</td>
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<td>20.0</td>
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<tr>
<td>471.omnetpp</td>
<td>10.3</td>
<td>19.6</td>
</tr>
<tr>
<td>473.astar</td>
<td>9.29</td>
<td></td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Hardware

CPU Name: Intel Xeon E5320
CPU Characteristics: 1.86 GHz, 2x4 MB L2 shared, 1066 MHz system bus
CPU MHz: 1860
FPU: Integrated
CPU(s) enabled: 4 cores, 1 chip, 4 cores/chip
CPU(s) orderable: 1,2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 8 MB I+D on chip per chip, 4 MB shared / 2 cores
L3 Cache: None
Other Cache: None
Memory: 16 GB (8x2 GB PC2-5300 CL5)
Disk Subsystem: 1x72 GB 10k SAS
Other Hardware: None

Software

Operating System: Windows Server 2003 Enterprise x64 Edition SP1
Compiler: Intel C++ Compiler for 32-bit applications, Version 9.1, Build 20061103Z
Package ID: W_CC_C_9.1.033
Microsoft Visual Studio .NET 2003 (v7.1.3088, for libraries)
Auto Parallel: No
File System: NTFS
System State: Default
Base Pointers: 32-bit
Peak Pointers: 32-bit
Other Software: MicroQuill SmartHeap Library 8.0
Hewlett-Packard Company
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```
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Platform Notes
Power Regulator set to Static High Performance Mode in BIOS.
Adjacent Sector Prefetch disabled in BIOS.

Base Compiler Invocation

C benchmarks:
icl -Qvc7.1 -Qc99

C++ benchmarks:
icl -Qvc7.1

Base Portability Flags

403.gcc: -DSPEC_CPU_WIN32
464.h264ref: -DSPEC_CPU_NO_INTTYPES -DWIN32

Base Optimization Flags

C benchmarks:
-fast /F512000000 shlw32m.lib -link /FORCE:MULTIPLE
### Hewlett-Packard Company

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## Base Optimization Flags (Continued)

**C++ benchmarks:**
```  
-fast -Qcxx_features /F512000000 shlw32m.lib  
-link /FORCE:MULTIPLE  
```

---

## Base Other Flags

**C benchmarks:**
```  
403.gcc: -Dalloca=_alloca  
```

---

## Peak Compiler Invocation

**C benchmarks:**
```  
icl -Qvc7.1 -Qc99  
```

**C++ benchmarks:**
```  
icl -Qvc7.1  
```

---

## Peak Portability Flags

```  
403.gcc: -DSPEC_CPU_WIN32  
464.h264ref: -DSPEC_CPU_NO_INTTYPES -DWIN32  
```

---

## Peak Optimization Flags

**C benchmarks:**
```  
400.perlbench: -Qprof_gen(pass 1) -Qprof_use(pass 2) -fast /F512000000  
shlw32m.lib -link /FORCE:MULTIPLE  
```

```  
401.bzip2: Same as 400.perlbench  
403.gcc: Same as 400.perlbench  
429.mcf: basepeak = yes  
445.gobmk: Same as 400.perlbench  
456.hmmer: Same as 400.perlbench  
458.sjeng: Same as 400.perlbench  
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Peak Optimization Flags (Continued)

462.libquantum: Same as 400.perlbench

464.h264ref: Same as 400.perlbench

C++ benchmarks:
- -Qprof_gen(pass 1) -Qprofile_use(pass 2) -fast -Qcxx_features
  /F512000000 shlw32m.lib

/Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags file that was used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/hp-ic91-flags.20090715.02.html

You can also download the XML flags source by saving the following link:
http://www.spec.org/cpu2006/flags/hp-ic91-flags.20090715.02.xml

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For other inquiries, please contact webmaster@spec.org.

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