SPEC® CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

ASUSTeK Computer Inc.

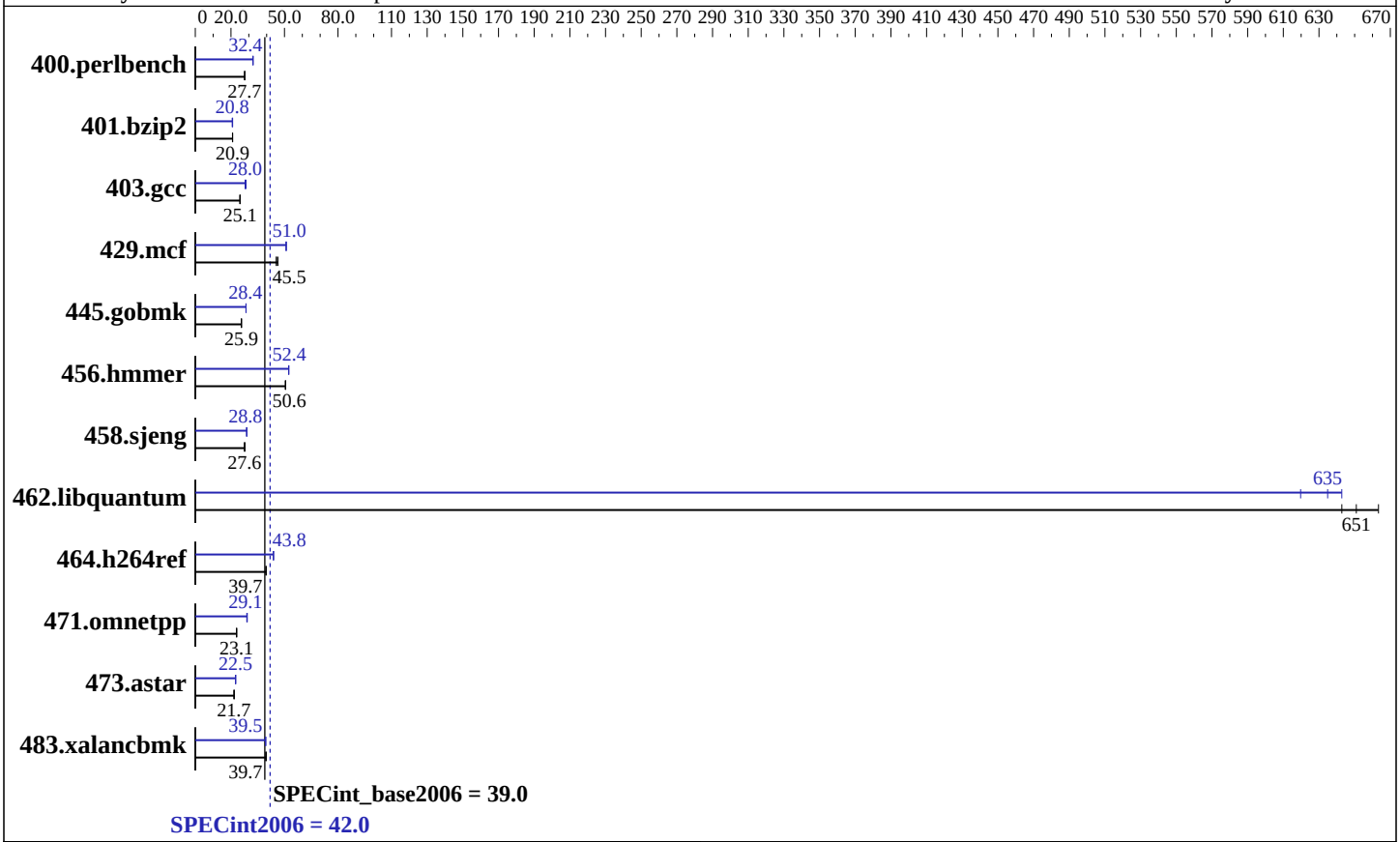
ASUS RS520-E6 (Z8NR-D12) server system
(Intel Xeon X5680)

SPECint®2006 = 42.0

SPECint_base2006 = 39.0

CPU2006 license: 9016
Test sponsor: ASUSTeK Computer Inc.
Tested by: ASUSTeK Computer Inc.

Test date: Jul-2010
Hardware Availability: Mar-2010
Software Availability: Jan-2010



Hardware

CPU Name:	Intel Xeon X5680
CPU Characteristics:	Intel Turbo Boost Technology up to 3.60 GHz
CPU MHz:	3333
FPU:	Integrated
CPU(s) enabled:	12 cores, 2 chips, 6 cores/chip, 2 threads/core
CPU(s) orderable:	1,2 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core
L3 Cache:	12 MB I+D on chip per chip
Other Cache:	None
Memory:	48 GB (12 x 4 GB PC3-10600R, CL=9)
Disk Subsystem:	HITACHI HDP725050GLA380 1 x 500 GB SATAII, 7200 RPM
Other Hardware:	None

Software

Operating System:	SUSE Linux Enterprise Server 11 (x86_64), Kernel 2.6.27.19-5-default
Compiler:	Intel C++ Professional Compiler for IA32 and Intel 64, Version 11.1 Build 20091130 Package ID: l_cproc_p_11.1.064
Auto Parallel:	Yes
File System:	ReiserFS
System State:	Run level 3 (multi-user)
Base Pointers:	64-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V8.1

SPEC CINT2006 Result

Copyright 2006-2014 Standard Performance Evaluation Corporation

ASUSTeK Computer Inc.

ASUS RS520-E6 (Z8NR-D12) server system
(Intel Xeon X5680)

SPECint2006 = 42.0

SPECint_base2006 = 39.0

CPU2006 license: 9016
Test sponsor: ASUSTeK Computer Inc.
Tested by: ASUSTeK Computer Inc.

Test date: Jul-2010
Hardware Availability: Mar-2010
Software Availability: Jan-2010

Results Table

Benchmark	Base						Peak					
	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	354	27.6	**353**	**27.7**	352	27.8	302	32.3	302	32.4	**302**	**32.4**
401.bzip2	463	20.8	**462**	**20.9**	461	20.9	**463**	**20.8**	466	20.7	461	20.9
403.gcc	**321**	**25.1**	320	25.1	322	25.0	288	27.9	**287**	**28.0**	283	28.5
429.mcf	197	46.3	**200**	**45.5**	201	45.4	**179**	**51.0**	179	51.0	179	50.9
445.gobmk	405	25.9	**405**	**25.9**	406	25.8	**369**	**28.4**	369	28.5	369	28.4
456.hmmer	**184**	**50.6**	185	50.4	184	50.7	178	52.4	178	52.4	**178**	**52.4**
458.sjeng	**439**	**27.6**	434	27.9	439	27.6	420	28.8	**420**	**28.8**	420	28.8
462.libquantum	**31.8**	**651**	31.2	663	32.2	643	32.2	643	**32.6**	**635**	33.4	620
464.h264ref	557	39.8	558	39.6	**558**	**39.7**	505	43.8	**505**	**43.8**	505	43.8
471.omnetpp	**270**	**23.1**	270	23.1	270	23.2	215	29.1	216	28.9	**215**	**29.1**
473.astar	321	21.9	324	21.7	**323**	**21.7**	309	22.7	**312**	**22.5**	312	22.5
483.xalancbmk	175	39.5	**174**	**39.7**	173	39.8	**175**	**39.5**	175	39.5	175	39.3

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

```
'ulimit -s unlimited' was used to set the stack size to unlimited prior to run
OMP_NUM_THREADS set to number of cores
KMP_AFFINITY set to granularity=fine,scatter
```

Component Notes

```
Tested system case compliance with Intel EEB 3.61 spec
SSI Server Power Supply 650W or higher
System was configured with ASPEED AST2050 VGA (on board VGA)
```

General Notes

```
Binaries were compiled on SLES 10 with Binutils 2.18.50.0.7.20080502
The ASUS RS500-E6 (Intel Xeon X5680, 3.33 GHz) and
the ASUS RS520-E6 (Intel Xeon X5680, 3.33 GHz) models are electronically equivalent.
The results have been measured on a ASUS RS520-E6 (Intel Xeon X5680, 3.33 GHz) model.
```

Base Compiler Invocation

C benchmarks:

```
icc  -m64
```

C++ benchmarks:

```
icpc -m64
```

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -static -parallel -opt-prefetch

C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs
-L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-64bit -lsmartheap64

Base Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64

400.perlbench: icc -m32

429.mcf: icc -m32

445.gobmk: icc -m32

464.h264ref: icc -m32

C++ benchmarks (except as noted below):
icpc -m32

Continued on next page

Peak Compiler Invocation (Continued)

473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -static(pass 2)
-prof-use(pass 2) -ansi-alias -opt-prefetch

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div -static(pass 2) -prof-use(pass 2)
-auto-ilp32 -opt-prefetch -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div -static -inline-calloc
-opt-malloc-options=3 -auto-ilp32

429.mcf: -xSSE4.2 -ipo -O3 -no-prec-div -static -opt-prefetch

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -O2
-ipo -no-prec-div -ansi-alias

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -static -unroll2
-ansi-alias -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -static(pass 2)
-prof-use(pass 2) -unroll4

462.libquantum: -xSSE4.2 -ipo -O3 -no-prec-div -static -parallel
-opt-prefetch -par-schedule-static=32768 -ansi-alias

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -static(pass 2)
-prof-use(pass 2) -unroll2 -ansi-alias

Continued on next page

Peak Optimization Flags (Continued)

C++ benchmarks:

471.omnetpp: `-xSSE4.2`(pass 2) `-prof-gen`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-prof-use`(pass 2) `-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs -L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-32bit -lsmartheap`

473.astar: `-xSSE4.2`(pass 2) `-prof-gen`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-prof-use`(pass 2) `-ansi-alias -opt-ra-region-strategy=routine -Wl,-z,muldefs -L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-64bit -lsmartheap64`

483.xalancbmk: `-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs -L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-32bit -lsmartheap`

Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags file that was used to format this result can be browsed at
`http://www.spec.org/cpu2006/flags/Intel-ic11.1-linux64-revF.20100609.html`

You can also download the XML flags source by saving the following link:
`http://www.spec.org/cpu2006/flags/Intel-ic11.1-linux64-revF.20100609.xml`

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.1.
Report generated on Wed Jul 23 11:16:57 2014 by SPEC CPU2006 PS/PDF formatter v6932.
Originally published on 20 July 2010.