Cisco Systems

Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

SPECint<sub>rate2006</sub> = 959
SPECint<sub>rate_base2006</sub> = 914

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware

- **CPU Name:** Intel Xeon E7-4850
- **CPU Characteristics:** Intel Turbo Boost Technology up to 2.40 GHz
- **CPU MHz:** 2000
- **FPU:** Integrated
- **CPU(s) enabled:** 40 cores, 4 chips, 10 cores/chip, 2 threads/core
- **CPU(s) orderable:** 1,2,3,4 chips
- **Primary Cache:** 32 KB I + 32 KB D on chip per core
- **Secondary Cache:** 256 KB I+D on chip per core
- **L3 Cache:** 24 MB I+D on chip per chip
- **Other Cache:** None
- **Memory:** 512 GB (32 x 16 GB 4Rx4 PC3-8500R-9, ECC)
- **Disk Subsystem:** 600 GB SAS 10K RPM
- **Other Hardware:** None

Software

- **Operating System:** Red Hat Enterprise Linux Server release 6.1 (Santiago)
- **Compiler:** C/C++: Version 12.1.0.225 of Intel C++ Studio XE for Linux
- **Auto Parallel:** No
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 32-bit
- **Peak Pointers:** 32/64-bit
- **Other Software:** Microquill SmartHeap V9.01
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Test date: Jan-2012
Hardware Availability: May-2011
Software Availability: Oct-2011

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>80</td>
<td>1095</td>
<td>714</td>
<td>1096</td>
<td>713</td>
<td>1092</td>
<td>715</td>
<td>80</td>
<td>931</td>
<td>840</td>
<td>937</td>
<td>834</td>
<td>936</td>
<td>835</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>80</td>
<td>1508</td>
<td>512</td>
<td>1507</td>
<td>512</td>
<td>1507</td>
<td>512</td>
<td>80</td>
<td>1442</td>
<td>535</td>
<td>1440</td>
<td>536</td>
<td>1450</td>
<td>532</td>
</tr>
<tr>
<td>403.gcc</td>
<td>80</td>
<td>913</td>
<td>706</td>
<td>915</td>
<td>704</td>
<td>913</td>
<td>706</td>
<td>80</td>
<td>920</td>
<td>700</td>
<td>916</td>
<td>703</td>
<td>911</td>
<td>707</td>
</tr>
<tr>
<td>429.mcf</td>
<td>80</td>
<td>574</td>
<td>1270</td>
<td>575</td>
<td>1270</td>
<td>574</td>
<td>1270</td>
<td>80</td>
<td>574</td>
<td>1270</td>
<td>575</td>
<td>1270</td>
<td>574</td>
<td>1270</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>80</td>
<td>1052</td>
<td>797</td>
<td>1051</td>
<td>798</td>
<td>1052</td>
<td>798</td>
<td>80</td>
<td>1004</td>
<td>836</td>
<td>1004</td>
<td>836</td>
<td>1003</td>
<td>836</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>80</td>
<td>678</td>
<td>1100</td>
<td>672</td>
<td>1110</td>
<td>672</td>
<td>1110</td>
<td>80</td>
<td>540</td>
<td>1380</td>
<td>540</td>
<td>1380</td>
<td>540</td>
<td>1380</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>80</td>
<td>1261</td>
<td>768</td>
<td>1261</td>
<td>768</td>
<td>1259</td>
<td>769</td>
<td>80</td>
<td>1169</td>
<td>828</td>
<td>1168</td>
<td>829</td>
<td>1168</td>
<td>829</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>80</td>
<td>296</td>
<td>5600</td>
<td>296</td>
<td>5600</td>
<td>296</td>
<td>5600</td>
<td>80</td>
<td>296</td>
<td>5600</td>
<td>296</td>
<td>5600</td>
<td>296</td>
<td>5600</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>80</td>
<td>1630</td>
<td>1090</td>
<td>1608</td>
<td>1100</td>
<td>1597</td>
<td>1110</td>
<td>80</td>
<td>1630</td>
<td>1090</td>
<td>1632</td>
<td>1080</td>
<td>1624</td>
<td>1090</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>80</td>
<td>971</td>
<td>515</td>
<td>971</td>
<td>515</td>
<td>969</td>
<td>516</td>
<td>80</td>
<td>919</td>
<td>544</td>
<td>919</td>
<td>544</td>
<td>921</td>
<td>543</td>
</tr>
<tr>
<td>473.astar</td>
<td>80</td>
<td>1098</td>
<td>511</td>
<td>1103</td>
<td>509</td>
<td>1096</td>
<td>513</td>
<td>80</td>
<td>1098</td>
<td>511</td>
<td>1103</td>
<td>509</td>
<td>1096</td>
<td>513</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>80</td>
<td>587</td>
<td>941</td>
<td>587</td>
<td>941</td>
<td>586</td>
<td>942</td>
<td>80</td>
<td>587</td>
<td>941</td>
<td>587</td>
<td>941</td>
<td>586</td>
<td>942</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
Sysinfo program /opt/cpu2006/config/sysinfo.rev6800
$Rev: 6800 $ $Date:: 2011-10-11 $ 6f2ebdf5f5032aaa42e583f96b07f99d3 running on localhost.localdomain Tue Jan 10 18:43:49 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E7- 4850 @ 2.00GHz
4 "physical id"s (chips)
80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20

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Platform Notes (Continued)

physical 0: cores 0 1 2 8 9 16 17 18 24 25
physical 1: cores 0 1 2 8 9 16 17 18 24 25
physical 2: cores 0 1 2 8 9 16 17 18 24 25
physical 3: cores 0 1 2 8 9 16 17 18 24 25
cache size : 24576 KB

From /proc/meminfo
MemTotal: 529231820 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.1 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.1 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.1 (Santiago)

uname -a:
Linux localhost.localdomain 2.6.32-131.0.15.el6.x86_64 #1 SMP Tue May 10 15:42:40 EDT 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 10 18:19

SPEC is set to: /opt/cpu2006
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 134G 5.8G 122G 5% /

Additional information from dmidecode:

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006/libs/32:/opt/cpu2006/libs/64"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RHEL5.5
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1 > /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
umactl --interleave=all runspec <etc>
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Base Compiler Invocation

C benchmarks:
  icc -m32
C++ benchmarks:
  icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
  -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
C++ benchmarks:
  -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
  -Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:
  403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
  icc -m32
  400.perlbench: icc -m64
  401.bzip2: icc -m64
  456.hmmer: icc -m64
  458.sjeng: icc -m64
C++ benchmarks:
  icpc -m32
Cisco Systems
Cisco UCS B440 M2 (Intel Xeon E7-4850, 2.00 GHz)

**SPECint**
\[ \text{SPECint}_{\text{rate}2006} = 959 \]
\[ \text{SPECint}_{\text{rate}_\text{base}2006} = 914 \]

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<thead>
<tr>
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<th>Test date:</th>
<th>Jan-2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test sponsor:</td>
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<td>Hardware Availability:</td>
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</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Oct-2011</td>
</tr>
</tbody>
</table>

**Peak Portability Flags**

- 400.perlbench: \(-\text{DSPEC\_CPU\_LP64}\) \(-\text{DSPEC\_CPU\_LINUX\_X64}\)
- 401.bzip2: \(-\text{DSPEC\_CPU\_LP64}\)
- 456.hmmer: \(-\text{DSPEC\_CPU\_LP64}\)
- 458.sjeng: \(-\text{DSPEC\_CPU\_LP64}\)
- 462.libquantum: \(-\text{DSPEC\_CPU\_LINUX}\)
- 483.xalancbmk: \(-\text{DSPEC\_CPU\_LINUX}\)

**Peak Optimization Flags**

**C benchmarks:**

- 400.perlbench: \(-\text{xSSE4.2}(\text{pass 2})\) \(-\text{prof-gen}(\text{pass 1})\) \(-\text{ipo}(\text{pass 2})\)
  \(-\text{o3}(\text{pass 2})\) \(-\text{no-prec-div}(\text{pass 2})\) \(-\text{prof-use}(\text{pass 2})\)
  \(-\text{auto-ilp32}\)

- 401.bzip2: \(-\text{xSSE4.2}(\text{pass 2})\) \(-\text{prof-gen}(\text{pass 1})\) \(-\text{ipo}(\text{pass 2})\)
  \(-\text{o3}(\text{pass 2})\) \(-\text{no-prec-div}(\text{pass 2})\) \(-\text{prof-use}(\text{pass 2})\)
  \(-\text{opt-prefetch}\) \(-\text{auto-ilp32}\) \(-\text{ansi-alias}\)

- 403.gcc: \(-\text{xSSE4.2}\) \(-\text{ipo}\) \(-\text{o3}\) \(-\text{no-prec-div}\)

- 429.mcf: \text{basepeak} = \text{yes}

- 445.gobmk: \(-\text{xSSE4.2}(\text{pass 2})\) \(-\text{prof-gen}(\text{pass 1})\) \(-\text{prof-use}(\text{pass 2})\)
  \(-\text{ansi-alias}\) \(-\text{opt-mem-layout-trans=3}\)

- 456.hmmer: \(-\text{xSSE4.2}\) \(-\text{ipo}\) \(-\text{o3}\) \(-\text{no-prec-div}\) \(-\text{unroll2}\) \(-\text{auto-ilp32}\)

- 458.sjeng: \(-\text{xSSE4.2}(\text{pass 2})\) \(-\text{prof-gen}(\text{pass 1})\) \(-\text{ipo}(\text{pass 2})\)
  \(-\text{o3}(\text{pass 2})\) \(-\text{no-prec-div}(\text{pass 2})\) \(-\text{prof-use}(\text{pass 2})\)
  \(-\text{unroll2}\) \(-\text{auto-ilp32}\)

- 462.libquantum: \text{basepeak} = \text{yes}

- 464.h264ref: \(-\text{xSSE4.2}(\text{pass 2})\) \(-\text{prof-gen}(\text{pass 1})\) \(-\text{ipo}(\text{pass 2})\)
  \(-\text{o3}(\text{pass 2})\) \(-\text{no-prec-div}(\text{pass 2})\) \(-\text{prof-use}(\text{pass 2})\)
  \(-\text{unroll2}\) \(-\text{ansi-alias}\)

**C++ benchmarks:**

- 471.omnetpp: \(-\text{xSSE4.2}(\text{pass 2})\) \(-\text{prof-gen}(\text{pass 1})\) \(-\text{ipo}(\text{pass 2})\)
  \(-\text{o3}(\text{pass 2})\) \(-\text{no-prec-div}(\text{pass 2})\) \(-\text{prof-use}(\text{pass 2})\)
  \(-\text{ansi-alias}\) \(-\text{opt-ra-region-strategy=block}\) \(-\text{Wl,-z,muldefs}\)
  \(-\text{L/smartheap}\) \(-\text{lsmartheap}\)

- 473.astar: \text{basepeak} = \text{yes}

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Peak Optimization Flags (Continued)

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.xml

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For other inquiries, please contact webmaster@spec.org.

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