Cisco Systems

Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

**SPECint**\_rate2006 = 439

**SPECint\_rate_base2006 = 419**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2006 license</td>
<td>9019</td>
</tr>
<tr>
<td>Test sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test date</td>
<td>Apr-2012</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Jun-2012</td>
</tr>
<tr>
<td>Software Availability</td>
<td>Dec-2011</td>
</tr>
</tbody>
</table>

### Hardware

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon E5-2630</td>
</tr>
<tr>
<td>CPU Characteristics</td>
<td>Intel Turbo Boost Technology up to 2.80 GHz</td>
</tr>
<tr>
<td>CPU MHz</td>
<td>2300</td>
</tr>
<tr>
<td>FPU</td>
<td>Integrated</td>
</tr>
<tr>
<td>CPU(s) enabled</td>
<td>12 cores, 2 chips, 6 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td>CPU(s) orderable</td>
<td>1.2 chip</td>
</tr>
<tr>
<td>Primary Cache</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Secondary Cache</td>
<td>256 KB I+D on chip per core</td>
</tr>
<tr>
<td>L3 Cache</td>
<td>15 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other Cache</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>128 GB (16 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1333 MHz and CL7)</td>
</tr>
<tr>
<td>Disk Subsystem</td>
<td>1 X 300 GB 10000 RPM SAS</td>
</tr>
<tr>
<td>Other Hardware</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System</td>
<td>Red Hat Enterprise Linux Server release 6.2 (Santiago) 2.6.32-220.el6.x86_64</td>
</tr>
<tr>
<td>Compiler</td>
<td>C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux</td>
</tr>
<tr>
<td>Auto Parallel</td>
<td>No</td>
</tr>
<tr>
<td>File System</td>
<td>ext4</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>32-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other Software</td>
<td>Microquill SmartHeap V9.01</td>
</tr>
</tbody>
</table>
Cisco Systems
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**SPEC CINT2006 Result**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Base</th>
<th>Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Seconds</td>
<td>Ratio</td>
</tr>
<tr>
<td>400.perlbench</td>
<td>24</td>
<td>770</td>
<td>305</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>24</td>
<td>1020</td>
<td>227</td>
</tr>
<tr>
<td>403.gcc</td>
<td>24</td>
<td>562</td>
<td>344</td>
</tr>
<tr>
<td>429.mcf</td>
<td>24</td>
<td>326</td>
<td>671</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>24</td>
<td>822</td>
<td>306</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>24</td>
<td>433</td>
<td>517</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>24</td>
<td>954</td>
<td>305</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>24</td>
<td>200</td>
<td>2480</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>24</td>
<td>1030</td>
<td>516</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>24</td>
<td>596</td>
<td>252</td>
</tr>
<tr>
<td>473.astar</td>
<td>24</td>
<td>673</td>
<td>250</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>24</td>
<td>351</td>
<td>471</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Platform Notes**

BIOS Configuration:
- Intel(R) Hyper-Threading Technology set to Enabled
- Processor Power State C6 set to Disabled
- Processor Power State C1 Enhanced set to Disabled
- Power Technology set to Custom
- Energy Performance set to Performance
- DRAM Clock Throttling set to Performance

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
$Rev:: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdff5032aaa42e583f96b07f99d3
running on localhost.localdomain Tue Apr  3 02:44:02 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) CPU E5-2630 0 @ 2.30GHz

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Cisco Systems

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CPU2006 license: 9019
Test sponsor: Cisco Systems
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Test date: Apr-2012
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Platform Notes (Continued)

2 "physical id"s (chips)
24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 6
siblings : 12
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
cache size : 15360 KB

From /proc/meminfo
MemTotal: 132101560 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.2 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)

uname -a:
Linux localhost.localdomain 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13 EST 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Apr 3 02:37

SPEC is set to: /opt/cpu2006-1.2

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 275G 9.9G 251G 4% /

Additional information from dmidecode:
Memory:
16x 0xCE00 M393B1K70DH0-YK0 8GB 1600 MHz 1 rank

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib32:/opt/cpu2006-1.2/lib64"

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
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Base Compiler Invocation

C benchmarks:
  icc  -m32
C++ benchmarks:
  icpc  -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
  -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
C++ benchmarks:
  -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
  -Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:
  403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
  icc  -m32
  400.perlbench: icc  -m64
  401.bzip2: icc  -m64
  456.hmmer: icc  -m64
  458.sjeng: icc  -m64
C++ benchmarks:
  icpc  -m32
Cisco Systems
Cisco UCS C220 M3 (Intel Xeon E5-2630, 2.30 GHz)

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SPECint_rate2006 = 439
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Peak Portability Flags
- 400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
- 401.bzip2: -DSPEC_CPU_LP64
- 456.hmmer: -DSPEC_CPU_LP64
- 458.sjeng: -DSPEC_CPU_LP64
- 462.libquantum: -DSPEC_CPU_LINUX
- 483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
- 400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -auto-ilkp32
- 401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -opt-prefetch -auto-ilkp32 -ansi-alias
- 403.gcc: -xSSE4.2 -ipo -o3 -no-prec-div
- 429.mcf: basepeak = yes
- 445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
  -ansi-alias -opt-mem-layout-trans=3
- 456.hmmer: -xSSE4.2 -ipo -o3 -no-prec-div -unroll2 -auto-ilkp32
- 458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll4 -auto-ilkp32
- 462.libquantum: basepeak = yes
- 464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll2 -ansi-alias

C++ benchmarks:
- 471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
  -L/smartheap -lsmartheap
- 473.astar: basepeak = yes

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Peak Optimization Flags (Continued)

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml

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For other inquiries, please contact webmaster@spec.org.