Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2665, 2.40 GHz)  

**SPECfp®2006 = 80.1**  

**SPECfp_base2006 = 76.9**

**Hardware**
- **CPU Name:** Intel Xeon E5-2665  
- **CPU Characteristics:** Intel Turbo Boost Technology up to 3.10 GHz  
- **CPU MHz:** 2400  
- **FPU:** Integrated  
- **CPU(s) enabled:** 16 cores, 2 chips, 8 cores/chip  
- **CPU(s) orderable:** 1.2 chip  
- **Primary Cache:** 32 KB I + 32 KB D on chip per core  
- **Secondary Cache:** 256 KB I+D on chip per core

**Software**
- **Operating System:** Red Hat Enterprise Linux Server release 6.2 (Santiago)  
- **Compiler:** C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux; Fortran: Version 12.1.3.293 of Intel Fortran Studio XE for Linux  
- **Auto Parallel:** Yes  
- **File System:** ext4

---

**Test sponsor:** Cisco Systems  
**Test date:** May-2012  
**Hardware Availability:** Jun-2012  
**Software Availability:** Dec-2011

---

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECfp2006</th>
<th>SPECfp_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>32.6</td>
<td>316</td>
</tr>
<tr>
<td>416.gamess</td>
<td>59.6</td>
<td></td>
</tr>
<tr>
<td>433.milc</td>
<td>59.0</td>
<td></td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>145</td>
<td></td>
</tr>
<tr>
<td>435.gromacs</td>
<td>34.9</td>
<td></td>
</tr>
<tr>
<td>436.cactusADM</td>
<td></td>
<td>442</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td></td>
<td>186</td>
</tr>
<tr>
<td>444.namd</td>
<td>21.4</td>
<td></td>
</tr>
<tr>
<td>447.dealII</td>
<td>51.2</td>
<td></td>
</tr>
<tr>
<td>450.soplex</td>
<td>39.1</td>
<td></td>
</tr>
<tr>
<td>453.povray</td>
<td>46.7</td>
<td></td>
</tr>
<tr>
<td>454.calculix</td>
<td>38.2</td>
<td></td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>465.tonto</td>
<td>39.3</td>
<td></td>
</tr>
<tr>
<td>470.lbm</td>
<td>34.6</td>
<td></td>
</tr>
<tr>
<td>481.wrf</td>
<td>73.2</td>
<td></td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>67.4</td>
<td></td>
</tr>
</tbody>
</table>

---

This report is a result of testing a Cisco UCS B200 M3 system equipped with an Intel Xeon E5-2665 processor. The system was tested using 16 cores, 2 chips, and 8 cores per chip. The primary cache is 32 KB I + 32 KB D on chip per core, and the secondary cache is 256 KB I+D on chip per core. The operating system used was Red Hat Enterprise Linux Server release 6.2 (Santiago), and the compiler was Intel C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux. Fortran was compiled using Version 12.1.3.293 of Intel Fortran Studio XE for Linux. The test was conducted in May 2012, with hardware availability in June and software availability in December of the same year. The result shows a SPECfp®2006 score of 80.1 and a SPECfp_base2006 score of 76.9.
**SPEC CFP2006 Result**

Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2665, 2.40 GHz)

**SPECfp2006 = 80.1**

**SPECfp_base2006 = 76.9**

**CPU2006 license:** 9019

**Test date:** May-2012

**Test sponsor:** Cisco Systems

**Hardware Availability:** Jun-2012

**Tested by:** Cisco Systems

**Software Availability:** Dec-2011

**L3 Cache:** 20 MB I+D on chip per chip

**System State:** Run level 3 (multi-user)

**Other Cache:** None

**Peak Pointers:** 32/64-bit

**Memory:** 128 GB (16 x 8 GB 2Rx4 PC3-12800R-11, ECC)

**Other Pointers:** Base Pointers: 64-bit

**Disk Subsystem:** 1 X 300 GB 10000 RPM SAS

**Other Software:** None

**Other Hardware:** None

**Base Pointers:** 64-bit

**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>43.0</td>
<td>316</td>
<td>43.2</td>
<td>314</td>
<td>42.8</td>
<td>317</td>
<td>44.0</td>
<td>309</td>
<td>44.4</td>
<td>306</td>
<td>43.2</td>
<td>314</td>
</tr>
<tr>
<td>416.gamess</td>
<td>681</td>
<td>28.7</td>
<td>680</td>
<td>28.8</td>
<td>682</td>
<td>28.7</td>
<td>600</td>
<td>32.6</td>
<td>601</td>
<td>32.6</td>
<td>600</td>
<td>32.6</td>
</tr>
<tr>
<td>433.mile</td>
<td>155</td>
<td>59.1</td>
<td>156</td>
<td>58.9</td>
<td>156</td>
<td>59.0</td>
<td>154</td>
<td>59.5</td>
<td>154</td>
<td>59.6</td>
<td>154</td>
<td>59.6</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>63.0</td>
<td>144</td>
<td>62.6</td>
<td>145</td>
<td>62.0</td>
<td>147</td>
<td>63.0</td>
<td>144</td>
<td>62.6</td>
<td>145</td>
<td>62.0</td>
<td>147</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>204</td>
<td>34.9</td>
<td>205</td>
<td>34.8</td>
<td>205</td>
<td>34.9</td>
<td>204</td>
<td>34.9</td>
<td>205</td>
<td>34.8</td>
<td>205</td>
<td>34.9</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>27.1</td>
<td>442</td>
<td>27.1</td>
<td>442</td>
<td>26.5</td>
<td>452</td>
<td>27.1</td>
<td>442</td>
<td>27.1</td>
<td>442</td>
<td>26.5</td>
<td>452</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>47.2</td>
<td>199</td>
<td>51.4</td>
<td>183</td>
<td>50.4</td>
<td>186</td>
<td>47.2</td>
<td>199</td>
<td>51.4</td>
<td>183</td>
<td>50.4</td>
<td>186</td>
</tr>
<tr>
<td>447.dealII</td>
<td>224</td>
<td>51.1</td>
<td>223</td>
<td>51.2</td>
<td>223</td>
<td>51.2</td>
<td>224</td>
<td>51.1</td>
<td>223</td>
<td>51.2</td>
<td>223</td>
<td>51.2</td>
</tr>
<tr>
<td>450.soplex</td>
<td>213</td>
<td>39.2</td>
<td>213</td>
<td>39.1</td>
<td>214</td>
<td>39.0</td>
<td>213</td>
<td>39.2</td>
<td>213</td>
<td>39.1</td>
<td>214</td>
<td>39.0</td>
</tr>
<tr>
<td>453.povray</td>
<td>135</td>
<td>39.5</td>
<td>135</td>
<td>39.4</td>
<td>135</td>
<td>39.3</td>
<td>114</td>
<td>46.7</td>
<td>114</td>
<td>46.6</td>
<td>112</td>
<td>47.7</td>
</tr>
<tr>
<td>454.calculix</td>
<td>235</td>
<td>35.2</td>
<td>233</td>
<td>35.4</td>
<td>235</td>
<td>35.1</td>
<td>216</td>
<td>38.2</td>
<td>214</td>
<td>38.5</td>
<td>216</td>
<td>38.2</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>79.1</td>
<td>134</td>
<td>79.5</td>
<td>134</td>
<td>79.5</td>
<td>134</td>
<td>66.3</td>
<td>160</td>
<td>66.3</td>
<td>160</td>
<td>66.9</td>
<td>158</td>
</tr>
<tr>
<td>465.tonto</td>
<td>285</td>
<td>34.6</td>
<td>284</td>
<td>34.6</td>
<td>284</td>
<td>34.6</td>
<td>284</td>
<td>34.6</td>
<td>284</td>
<td>34.6</td>
<td>284</td>
<td>34.6</td>
</tr>
<tr>
<td>470.lbm</td>
<td>34.0</td>
<td>404</td>
<td>38.2</td>
<td>360</td>
<td>35.6</td>
<td>386</td>
<td>34.0</td>
<td>404</td>
<td>38.2</td>
<td>360</td>
<td>35.6</td>
<td>386</td>
</tr>
<tr>
<td>481.wrf</td>
<td>154</td>
<td>72.7</td>
<td>153</td>
<td>73.2</td>
<td>152</td>
<td>73.4</td>
<td>154</td>
<td>72.7</td>
<td>153</td>
<td>73.2</td>
<td>152</td>
<td>73.4</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>289</td>
<td>67.4</td>
<td>291</td>
<td>67.0</td>
<td>285</td>
<td>68.3</td>
<td>289</td>
<td>67.4</td>
<td>291</td>
<td>67.0</td>
<td>285</td>
<td>68.3</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Platform Notes**

BIOS Configuration:
- Processor C6 Report set to Disabled
- Processor CIE set to Disabled
- CPU Performance set to HPC
- LV DDR Mode set to Performance
- Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
  $$Rev: 6800 $$ $$Date:: 2011-10-11 $$ 6f2e6bdf5032aa42e583f96b07f99d3
  running on localhost.localdomain Tue May 1 19:16:47 2012

This section contains SUT (System Under Test) info as seen by
Continued on next page

Standard Performance Evaluation Corporation
info@spec.org
http://www.spec.org/
Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2665, 2.40 GHz)

SPECfp2006 = 80.1
SPECfp_base2006 = 76.9

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2012
Hardware Availability: Jun-2012
Software Availability: Dec-2011

Platform Notes (Continued)

some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) CPU E5-2665 0 @ 2.40GHz
  2 "physical id"s (chips)
  16 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The
  following excerpts from /proc/cpuinfo might not be reliable. Use with
  caution.)
    cpu cores : 8
    siblings : 8
    physical 0: cores 0 1 2 3 4 5 6 7
    physical 1: cores 0 1 2 3 4 5 6 7
  cache size : 20480 KB

From /proc/meminfo
  MemTotal: 132101936 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
  Red Hat Enterprise Linux Server release 6.2 (Santiago)

From /etc/*release* /etc/*version*
  redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
  system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)

uname -a:
  Linux localhost.localdomain 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13
  EST 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 1 19:10

SPEC is set to: /opt/cpu2006-1.2
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda1 ext4 275G 8.0G 253G 4% /

Additional information from dmidecode:
  Memory:
    16x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 1 rank

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"
OMP_NUM_THREADS = "16"

Continued on next page
## SPEC CFP2006 Result

**Cisco Systems**

Cisco UCS B200 M3 (Intel Xeon E5-2665, 2.40 GHz)

### SPECfp2006 = 80.1

### SPECfp_base2006 = 76.9

<table>
<thead>
<tr>
<th>CPU2006 license: 9019</th>
<th>Test date: May-2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test sponsor: Cisco Systems</td>
<td>Hardware Availability: Jun-2012</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Dec-2011</td>
</tr>
</tbody>
</table>

### General Notes (Continued)

Intel HT Technology = disable  
Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2  
Transparent Huge Pages enabled with:  
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled  
Filesystem page cache cleared with:  
echo 1> /proc/sys/vm/drop_caches

### Base Compiler Invocation

<table>
<thead>
<tr>
<th>C benchmarks:</th>
<th>icc -m64</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++ benchmarks:</td>
<td>icpc -m64</td>
</tr>
<tr>
<td>Fortran benchmarks:</td>
<td>ifort -m64</td>
</tr>
<tr>
<td>Benchmarks using both Fortran and C:</td>
<td>icc -m64 ifort -m64</td>
</tr>
</tbody>
</table>

### Base Portability Flags

- 410.bwaves: -DSPEC_CPU_LP64
- 416.gamess: -DSPEC_CPU_LP64
- 433.milc: -DSPEC_CPU_LP64
- 434.zeusmp: -DSPEC_CPU_LP64
- 435.gromacs: -DSPEC_CPU_LP64 -nofor_main
- 436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
- 437.leslie3d: -DSPEC_CPU_LP64
- 444.namd: -DSPEC_CPU_LP64
- 447.dealII: -DSPEC_CPU_LP64
- 450.soplex: -DSPEC_CPU_LP64
- 453.povray: -DSPEC_CPU_LP64
- 454.calculix: -DSPEC_CPU_LP64 -nofor_main
- 459.GemsFDTD: -DSPEC_CPU_LP64
- 465.tonto: -DSPEC_CPU_LP64
- 470.lbm: -DSPEC_CPU_LP64
- 481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
- 482.sphinx3: -DSPEC_CPU_LP64

### Base Optimization Flags

- C benchmarks:  
  -xAVX -ipo -O3 -no-prec-div -static -parallel -opt-prefetch  
  -ansi-alias

Continued on next page
Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2665, 2.40 GHz)

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Base Optimization Flags (Continued)

C++ benchmarks:
-xAVX  -ipo  -O3  -no-prec-div  -static  -opt-prefetch  -ansi-alias

Fortran benchmarks:
-xAVX  -ipo  -O3  -no-prec-div  -static  -parallel  -opt-prefetch

Benchmarks using both Fortran and C:
-xAVX  -ipo  -O3  -no-prec-div  -static  -parallel  -opt-prefetch
-ansi-alias

Peak Compiler Invocation

C benchmarks:
   icc   -m64

C++ benchmarks:
   icpc  -m64

Fortran benchmarks:
   ifort -m64

Benchmarks using both Fortran and C:
   icc  -m64 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
   433.milc: -xAVX(pass 2)  -prof-gen(pass 1)  -ipo(pass 2)  -O3(pass 2)
   -no-prec-div(pass 2)  -prof-use(pass 2)  -static  -auto-ilp32
   -ansi-alias

   470.lbm: basepeak = yes

   482.sphinx3: basepeak = yes

C++ benchmarks:
   444.namd: -xAVX(pass 2)  -prof-gen(pass 1)  -ipo(pass 2)  -O3(pass 2)
   -no-prec-div(pass 2)  -prof-use(pass 2)  -fno-alias
   -auto-ilp32

Continued on next page
Cisco Systems

Cisco UCS B200 M3 (Intel Xeon E5-2665, 2.40 GHz)

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Spec CFP2006 Result
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Peak Optimization Flags (Continued)

447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -03(pass 2)
            -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
410.bwaves: -xAVX -ipo -03 -no-prec-div -opt-prefetch -parallel
            -static
416.gamess: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -03(pass 2)
            -no-prec-div(pass 2) -prof-use(pass 2) -unroll2
            -inline-level=0 -scalar-rep -static
434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes
459.GemsFDTD: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -03(pass 2)
            -no-prec-div(pass 2) -prof-use(pass 2) -unroll2
            -inline-level=0 -opt-prefetch -parallel
465.tonto: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -03(pass 2)
            -no-prec-div(pass 2) -prof-use(pass 2) -inline-calloc
            -opt-malloc-options=3 -auto -unroll4

Benchmarks using both Fortran and C:
435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes
454.calculix: -xAVX -ipo -03 -no-prec-div -auto-ilp32 -ansi-alias
481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml
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For questions about this result, please contact the tester. For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.  