Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2650, 2.00 GHz)

| SPECint®2006 = | 45.3 |
| SPECint_base2006 = | 41.9 |

- CPU2006 license: 9019
- Test date: May-2012
- Tested by: Cisco Systems
- Hardware Availability: Jun-2012
- Test sponsor: Cisco Systems
- Software Availability: Dec-2011

### Hardware

| CPU Name: Intel Xeon E5-2650 |
| CPU Characteristics: Intel Turbo Boost Technology up to 2.80 GHz |
| CPU MHz: 2000 |
| FPU: Integrated |
| CPU(s) enabled: 16 cores, 2 chips, 8 cores/chip |
| CPU(s) orderable: 1.2 chip |
| Primary Cache: 32 KB I + 32 KB D on chip per core |
| Secondary Cache: 256 KB I+D on chip per core |
| L3 Cache: 20 MB I+D on chip per chip |
| Other Cache: None |
| Memory: 128 GB (16 x 8 GB 2Rx4 PC3-12800R-11, ECC) |
| Disk Subsystem: 1 X 600 GB 10000 RPM SAS |
| Other Hardware: None |

### Software

| Operating System: Red Hat Enterprise Linux Server release 6.2 (Santiago) |
| Compiler: C/C++ Version 12.1.3.293 of Intel C++ StudioXE |
| Auto Parallel: Yes |
| File System: ext4 |
| System State: Run level 3 (multi-user) |
| Base Pointers: 32/64-bit |
| Peak Pointers: 32/64-bit |
| Other Software: Microquill SmartHeap V9.01 |
SPEC CINT2006 Result

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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds Base</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds Base</th>
<th>Ratio</th>
<th>Seconds Peak</th>
<th>Ratio</th>
<th>Seconds</th>
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<td>25.1</td>
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<td>331</td>
<td>29.5</td>
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<tr>
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<td>18.7</td>
<td>516</td>
<td>18.7</td>
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<td>483.xalancbmk</td>
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<td>43.1</td>
<td>154</td>
<td>44.7</td>
<td>155</td>
<td>44.6</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Configuration:
Processor Power State C6 set to Disabled
Processor Power State C1 Enhanced set to Disabled
Power Technology set to Custom
Energy Performance set to Performance
DRAM Clock Throttling set to Performance

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
$Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdf5032aaa42e583f96b07f99d3
running on localhost.localdomain Mon May  7 15:17:55 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2650 0 @ 2.00GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8

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Cisco Systems

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### Platform Notes (Continued)

- physical 0: cores 0 1 2 3 4 5 6 7
- physical 1: cores 0 1 2 3 4 5 6 7
- cache size : 20480 KB

From `/proc/meminfo`
- MemTotal: 132102596 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/usr/bin/lsb_release -d`
- Red Hat Enterprise Linux Server release 6.2 (Santiago)

From `/etc/*release* /etc/*version*`
- redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
- system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)

unname -a:
- Linux localhost.localdomain 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13 EST 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 7 14:54

SPEC is set to: `/opt/cpu2006-1.2`

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 550G 9.9G 512G 2% /

Additional information from dmidecode:
- Memory:
  - 16x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 1 rank

(End of data from sysinfo program)

---

### General Notes

- Environment variables set by runspec before the start of the run:
  - KMP_AFFINITY = "granularity=fine,scatter"
  - LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"
  - OMP_NUM_THREADS = "16"
  - Intel HT Technology = disable

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2

Transparent Huge Pages enabled with:
- echo always > /sys/kernel/mm/redhat_transparent_hugepage(enabled
- Filesystem page cache cleared with:
- echo 1> /proc/sys/vm/drop_caches

---
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Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32

C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-Wl,-z,muldefs -L/smartheap -lsmartheap64

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64

Continued on next page
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Peak Compiler Invocation (Continued)

400.perlbench: icc -m32
445.gobmk: icc -m32
464.h264ref: icc -m32
C++ benchmarks (except as noted below):
icpc -m32
473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -ansi-alias

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-o3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32
-opt-prefetch -ansi-alias

403.gcc: -xSSE4.2 -ipo -o3 -no-prec-div -inline-calloc
-opt-malloc-options=3 -auto-ilp32

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias

456.hmmer: -xSSE4.2 -ipo -o3 -no-prec-div -unroll2 -auto-ilp32
-ansi-alias

Continued on next page
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Peak Optimization Flags (Continued)

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

Peak Other Flags

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-ra-region-strategy=block -ansi-alias
-Wl,-z,muldefs -L/smartheap -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: -xSSE4.2 -ipo -03 -no-prec-div -opt-prefetch -ansi-alias
-Wl,-z,muldefs -L/smartheap -lsmartheap

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml

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For other inquiries, please contact webmaster@spec.org.

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