Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2609, 2.40 GHz)

SPECfp®2006 = 59.9
SPECfp_base2006 = 58.1

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Software
Operating System: Red Hat Enterprise Linux Server release 6.2 (Santiago)
Compiler: C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux;
Fortran: Version 12.1.3.293 of Intel Fortran Studio XE for Linux
Auto Parallel: Yes
File System: ext4

Hardware
CPU Name: Intel Xeon E5-2609
CPU Characteristics:
CPU MHz: 2400
FPU: Integrated
CPU(s) enabled: 8 cores, 2 chips, 4 cores/chip
CPU(s) orderable: 1.2 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core

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Cisco Systems

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CPU2006 license: 9019
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L3 Cache: 10 MB I+D on chip per chip
Other Cache: None
Memory: 128 GB (16 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1067 MHz and CL7)
Disk Subsystem: 1 X 600 GB 10000 RPM SAS
Other Hardware: None
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other Software: None

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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Configuration:
Intel(R) Hyper-Threading Technology set to Disabled
Processor Power State C6 set to Disabled
Processor Power State C1 Enhanced set to Disabled
Power Technology set to Custom
Energy Performance set to Performance
DRAM Clock Throttling set to Performance
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
$Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdfff5032aaa42e583f96b07f99d3
Continued on next page
Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2609, 2.40 GHz)

SPECfp2006 = 59.9
SPECfp_base2006 = 58.1

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2012
Hardware Availability: Jun-2012
Software Availability: Dec-2011

Platform Notes (Continued)


This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2609 0 @ 2.40GHz
2 "physical id"s (chips)
8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4
physical 0: cores 0 1 2 3
physical 1: cores 0 1 2 3
cache size : 10240 KB

From /proc/meminfo
MemTotal: 132103588 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.2 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.2 (Santiago)

uname -a:
Linux localhost.localdomain 2.6.32-220.el6.x86_64 #1 SMP Wed Nov 9 08:03:13 EST 2011 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 16 22:24

SPEC is set to: /opt/cpu2006-1.2

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 550G 9.9G 512G 2% /

Additional information from dmidecode:
Memory:
16x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 1 rank

(End of data from sysinfo program)
Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2609, 2.40 GHz)

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**General Notes**

Environment variables set by runspec before the start of the run:

- `KMP_AFFINITY = "granularity=fine,scatter"
- `LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"
- `OMP_NUM_THREADS = "8"

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2

Transparent Huge Pages enabled with:

```
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
```

Filesystem page cache cleared with:

```
echo 1> /proc/sys/vm/drop_caches
```

**Base Compiler Invocation**

C benchmarks:

```
icc -m64
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

Benchmarks using both Fortran and C:

```
icc -m64 ifort -m64
```

**Base Portability Flags**

```
410.bwaves: -DSPEC_CPU_LP64
416.games: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64
```
Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2609, 2.40 GHz)

SPECfp2006 = 59.9
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Base Optimization Flags

C benchmarks:
-xAVX -ipo -O3 -no-prec-div -static -parallel -opt-prefetch
-ansi-alias

C++ benchmarks:
-xAVX -ipo -O3 -no-prec-div -static -opt-prefetch -ansi-alias

Fortran benchmarks:
-xAVX -ipo -O3 -no-prec-div -static -parallel -opt-prefetch

Benchmarks using both Fortran and C:
-xAVX -ipo -O3 -no-prec-div -static -parallel -opt-prefetch
-ansi-alias

Peak Compiler Invocation

C benchmarks:
icc   -m64

C++ benchmarks:
icpc  -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc   -m64 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

433.milc: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -prof-use(pass 2) -static -auto-ilp32
-ansi-alias

470.lbm: basepeak = yes

482.sphinx3: basepeak = yes

Continued on next page
Cisco Systems  
Cisco UCS C240 M3 (Intel Xeon E5-2609, 2.40 GHz)  
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Peak Optimization Flags (Continued)

C++ benchmarks:

444.namd: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) 
-no-prec-div(pass 2) -prof-use(pass 2) -fno-alias 
-auto-ilp32

447.dealII: basepeak = yes

450.soplex: basepeak = yes

453.povray: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) 
-no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:

410.bwaves: -xAVX -ipo -O3 -no-prec-div -opt-prefetch -parallel 
-static

416.gamess: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) 
-no-prec-div(pass 2) -prof-use(pass 2) -unroll2 
-inline-level=0 -scalar-rep- -static

434.zeusmp: basepeak = yes

437.leslie3d: basepeak = yes

459.GemsFDTD: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) 
-no-prec-div(pass 2) -prof-use(pass 2) -unroll2 
-inline-level=0 -opt-prefetch -parallel

465.tonto: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) 
-no-prec-div(pass 2) -prof-use(pass 2) -inline-calloc 
-opt-malloc-options=3 -auto -unroll4

Benchmarks using both Fortran and C:

435.gromacs: basepeak = yes

436.cactusADM: basepeak = yes

454.calculix: -xAVX -ipo -O3 -no-prec-div -auto-ilp32 -ansi-alias

481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at  
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html  
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html
## SPEC CFP2006 Result

### Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2609, 2.40 GHz)

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You can also download the XML flags sources by saving the following links:

- [Intel-ic12.1-official-linux64.20111122.xml](http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml)
- [Cisco-Platform-Settings-V1.2.20130607.xml](http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml)

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For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.


Originally published on 5 June 2012.