Dell Inc. PowerEdge R520 (Intel Xeon E5-2450, 2.10 GHz)

<table>
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<th>SPECint_rate_base2006</th>
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<td>546</td>
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</table>

CPU2006 license: 55
Test sponsor: Dell Inc.
Tested by: Dell Inc.

CPU Name: Intel Xeon E5-2450
CPU Characteristics: Intel Turbo Boost Technology up to 2.90 GHz
CPU MHz: 2100
FPU: Integrated
CPU(s) enabled: 16 cores, 2 chips, 8 cores/chip, 2 threads/core
CPU(s) orderable: 1.2 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 20 MB I+D on chip per chip
Other Cache: None
Memory: 48 GB (6 x 8 GB 2Rx4 PC3-12800R-11, ECC)
Disk Subsystem: 2 x 600 GB 15000 RPM SAS, RAID 1
Other Hardware: None

Operating System: SUSE Linux Enterprise Server 11 SP2 (x86_64) 3.0.13-0.9-default
Compiler: C/C++: Version 12.1.0.225 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: ext3
System State: Run level 3 (add definition here)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V9.01

Software

Hardware

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<table>
<thead>
<tr>
<th>SPECint_rate_base2006</th>
<th>525</th>
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<tbody>
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</table>

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Standard Performance Evaluation Corporation
info@spec.org
http://www.spec.org/
Dell Inc.  
PowerEdge R520 (Intel Xeon E5-2450, 2.10 GHz)  

**SPEC CINT2006 Result**

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<td>434</td>
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**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Platform Notes**

CPU Power Management set to Maximum Performance
Memory Frequency set to Maximum Performance
Turbo Boost set to Enabled
C States/C1E set to Enabled
Sysinfo program /root/CPU2006-1.2/config/sysinfo.rev6800
$Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdff5032aaa42e583f96b07f99d3
running on Silk-2P Fri Apr 27 13:34:42 2012

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2450 0 @ 2.10GHz
  2 "physical id"s (chips)
  32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The Continued on next page
SPEC CINT2006 Result

Dell Inc.

PowerEdge R520 (Intel Xeon E5-2450, 2.10 GHz)

SPECint_rate2006 = 546
SPECint_rate_base2006 = 525

CPU2006 license: 55
Test sponsor: Dell Inc.
Tested by: Dell Inc.

Platform Notes (Continued)

following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

  cpu cores : 8
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7
  physical 1: cores 0 1 2 3 4 5 6 7
  cache size : 20480 KB

From /proc/meminfo
  MemTotal: 49381468 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
  SUSE Linux Enterprise Server 11 (x86_64)

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 11 (x86_64)
    VERSION = 11
    PATCHLEVEL = 2

uname -a:
  Linux Silk-2P 3.0.13-0.9-default #1 SMP Mon Jan 16 17:33:03 UTC 2012
    (54ddfaf) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Apr 27 13:33 last=S

SPEC is set to: /root/CPU2006-1.2
  Filesystem     Type  Size  Used Avail Use% Mounted on
  /dev/sda1      ext3  493G  7.4G  460G   2% /

Additional information from dmidecode:

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/root/CPU2006-1.2/libs/32:/root/CPU2006-1.2/libs/64"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RHEL5.5
Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
  echo 1>/proc/sys/vm/drop_caches
runcspec command invoked through numactl i.e.:
  numactl --interleave=all runspec <etc>
The Dell PowerEdge R520 and the Bull NovaScale R450 F3 models are electronically equivalent.

Continued on next page
General Notes (Continued)

The results have been measured on a Dell PowerEdge R520 model.

---

**Base Compiler Invocation**

C benchmarks:
- icc -m32

C++ benchmarks:
- icpc -m32

---

**Base Portability Flags**

- 400.perlbench: -DSPEC_CPU_LINUX_IA32
- 462.libquantum: -DSPEC_CPU_LINUX
- 483.xalancbmk: -DSPEC_CPU_LINUX

---

**Base Optimization Flags**

C benchmarks:
- -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:
- -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
- -Wl,-z,muldefs -L/smartheap -lsmartheap

---

**Base Other Flags**

C benchmarks:
- 403.gcc: -Dalloca=_alloca

---

**Peak Compiler Invocation**

C benchmarks (except as noted below):
- icc -m32

- 400.perlbench: icc -m64
- 401.bzip2: icc -m64
- 456.hmmer: icc -m64

Continued on next page
Dell Inc.

PowerEdge R520 (Intel Xeon E5-2450, 2.10 GHz)

 SPECint_rate2006 = 546
 SPECint_rate_base2006 = 525

CPU2006 license: 55
Test sponsor: Dell Inc.
Tested by: Dell Inc.

Peak Compiler Invocation (Continued)

458.sjeng: icc -m64

C++ benchmarks:
icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias
Dell Inc.
PowerEdge R520 (Intel Xeon E5-2450, 2.10 GHz)

SPECint_rate2006 = 546
SPECint_rate_base2006 = 525

CPU2006 license: 55
Test sponsor: Dell Inc.
Test date: Apr-2012
Tested by: Dell Inc.
Hardware Availability: May-2012
Software Availability: Feb-2012

Peak Optimization Flags (Continued)

C++ benchmarks:

    471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
               -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
               -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
               -L/smartheap -lsmartheap

    473.astar: basepeak = yes

    483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

    403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.html
http://www.spec.org/cpu2006/flags/Dell-Platform-Settings-V1.2-revA.20120410.00.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20111122.xml
http://www.spec.org/cpu2006/flags/Dell-Platform-Settings-V1.2-revA.20120410.00.xml

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For other inquiries, please contact webmaster@spec.org.

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