Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4607, 2.20 GHz)

SPECint®2006 = 33.2
SPECint_base2006 = 31.4

Hardware

CPU Name: Intel Xeon E5-4607
CPU Characteristics:
CPU MHZ: 2200
FPU: Integrated
CPU(s) enabled: 24 cores, 4 chips, 6 cores/chip
CPU(s) orderable: 1,2,3,4 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 12 MB I+D on chip per chip
Other Cache: None
Memory: 256 GB (32 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1066 MHz and CL7)
Disk Subsystem: 1 X 600 GB 10000 RPM SAS
Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.2 (Santiago)
Compiler: C/C++ Version 12.1.3.293 of Intel C++ Studio XE for Linux
Auto Parallel: Yes
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V9.01
Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4607, 2.20 GHz)

**SPECint2006 = 33.2**

**SPECint_base2006 = 31.4**

---

**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test date:** Feb-2013  
**Hardware Availability:** Nov-2012  
**Software Availability:** Feb-2012

---

**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>510</td>
<td>19.1</td>
<td>512</td>
<td>19.1</td>
<td>508</td>
<td>19.2</td>
<td>431</td>
<td>22.6</td>
<td>429</td>
<td>22.8</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>662</td>
<td>14.6</td>
<td>662</td>
<td>14.6</td>
<td>662</td>
<td>14.6</td>
<td>649</td>
<td>14.9</td>
<td>649</td>
<td>14.9</td>
</tr>
<tr>
<td>403.mcf</td>
<td>421</td>
<td>19.1</td>
<td>421</td>
<td>19.1</td>
<td>421</td>
<td>19.1</td>
<td>419</td>
<td>19.2</td>
<td>420</td>
<td>19.1</td>
</tr>
<tr>
<td>429.mcf</td>
<td>228</td>
<td>40.0</td>
<td>226</td>
<td>40.3</td>
<td>229</td>
<td>39.9</td>
<td>228</td>
<td>40.0</td>
<td>226</td>
<td>40.3</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>672</td>
<td>15.6</td>
<td>672</td>
<td>15.6</td>
<td>673</td>
<td>15.6</td>
<td>638</td>
<td>16.4</td>
<td>638</td>
<td>16.4</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>277</td>
<td>33.7</td>
<td>277</td>
<td>33.7</td>
<td>277</td>
<td>33.7</td>
<td>270</td>
<td>34.5</td>
<td>270</td>
<td>34.5</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>698</td>
<td>17.3</td>
<td>698</td>
<td>17.3</td>
<td>697</td>
<td>17.4</td>
<td>697</td>
<td>17.4</td>
<td>697</td>
<td>17.4</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>11.9</td>
<td>1740</td>
<td>11.7</td>
<td>1770</td>
<td><strong>11.7</strong></td>
<td><strong>1770</strong></td>
<td>11.9</td>
<td>1740</td>
<td>11.7</td>
<td>1770</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>709</td>
<td>31.2</td>
<td>719</td>
<td>30.8</td>
<td><strong>710</strong></td>
<td><strong>31.2</strong></td>
<td>637</td>
<td>34.7</td>
<td>637</td>
<td>34.7</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>433</td>
<td>14.4</td>
<td><strong>433</strong></td>
<td><strong>14.4</strong></td>
<td>433</td>
<td>14.4</td>
<td>343</td>
<td>18.2</td>
<td>343</td>
<td>18.2</td>
</tr>
<tr>
<td>473.astar</td>
<td><strong>374</strong></td>
<td><strong>18.7</strong></td>
<td>376</td>
<td>18.7</td>
<td>374</td>
<td>18.8</td>
<td><strong>374</strong></td>
<td><strong>18.7</strong></td>
<td>376</td>
<td>18.7</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>221</td>
<td>31.2</td>
<td><strong>221</strong></td>
<td><strong>31.2</strong></td>
<td>225</td>
<td>30.6</td>
<td>208</td>
<td>33.2</td>
<td>208</td>
<td>33.2</td>
</tr>
</tbody>
</table>

---

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

---

**Platform Notes**

BIOS Configuration:  
Processor Power State C6 set to Disabled  
Processor Power State C1 Enhanced set to Disabled  
Power Technology set to Custom  
Energy Performance set to Performance  
DRAM Clock Throttling set to Performance  
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800  
$Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdff5032aaa42e583f96b07f99d3  
running on localhost.localdomain Thu Feb 28 00:23:42 2013

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:  
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) CPU E5-4607 0 @ 2.20GHz  
4 "physical id"s (chips)  
24 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores: 6  
siblings: 6

---

Continued on next page
Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4607, 2.20 GHz)

SPECint2006 = 33.2
SPECint_base2006 = 31.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Feb-2013
Hardware Availability: Nov-2012
Software Availability: Feb-2012

Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
physical 2: cores 0 1 2 3 4 5
physical 3: cores 0 1 2 3 4 5

cache size : 12288 KB

MemTotal: 529256772 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/unr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.2 (Santiago)

Additional information from dmidecode:

Memory:
32x 0xCE00 M393B2G70BH0-YK0 16 GB 1600 MHz 2 rank

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"
OMP_NUM_THREADS = "24"

Intel HT Technology=disable

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2

Transparent Huge Pages enabled with:
    echo always > /sys/kernel/mm/redhat_transparent_hugepage/enable

Filesystem page cache cleared with:
    echo 1 > /proc/sys/vm/drop_caches
Cisco Systems
Cisco UCS C420 M3 (Intel Xeon E5-4607, 2.20 GHz)

SPECint2006 = 33.2
SPECint_base2006 = 31.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Feb-2013
Hardware Availability: Nov-2012
Software Availability: Feb-2012

Base Compiler Invocation

C benchmarks:
  icc  -m64

C++ benchmarks:
  icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
 403.gcc: -DSPEC_CPU_LP64
 429.mcf: -DSPEC_CPU_LP64
 445.gobmk: -DSPEC_CPU_LP64
 456.hmmer: -DSPEC_CPU_LP64
 458.sjeng: -DSPEC_CPU_LP64
 462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
 464.h264ref: -DSPEC_CPU_LP64
 471.omnetpp: -DSPEC_CPU_LP64
 473.astar: -DSPEC_CPU_LP64
 483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
  -xsSE4.2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32

C++ benchmarks:
  -xsSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
  -Wl,-z,muldefs -L/smartheap -lsmartheap64

Base Other Flags

C benchmarks:
  403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
  icc  -m64

Continued on next page
## Cisco UCS C420 M3 (Intel Xeon E5-4607, 2.20 GHz)

**SPECint2006 =** 33.2  
**SPECint_base2006 =** 31.4

### CPU2006 license: 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test date:** Feb-2013  
**Hardware Availability:** Nov-2012  
**Software Availability:** Feb-2012

---

### Peak Compiler Invocation (Continued)

400.perlbench:icc  
445.gobmk:icc  
464.h264ref:icc

C++ benchmarks (except as noted below):

icpc  
473.astar:icpc

---

### Peak Portability Flags

400.perlbench:-DSPEC_CPU_LINUX_IA32  
401.bzip2:-DSPEC_CPU_LP64  
403.gcc:-DSPEC_CPU_LP64  
429.mcf:-DSPEC_CPU_LP64  
456.hmmer:-DSPEC_CPU_LP64  
458.sjeng:-DSPEC_CPU_LP64  
462.libquantum:-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX  
473.astar:-DSPEC_CPU_LP64  
483.xalancbmk:-DSPEC_CPU_LINUX

---

### Peak Optimization Flags

**C benchmarks:**

400.perlbench:-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
-x3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)  
-opt-prefetch -ansi-alias

401.bzip2:-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
-x3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32  
-opt-prefetch -ansi-alias

403.gcc:-xSSE4.2 -ipo -x3 -no-prec-div -inline-calloc  
-opt-malloc-options=3 -auto-ilp32

429.mcf:basepeak = yes

445.gobmk:-xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)  
-ansi-alias

456.hmmer:-xSSE4.2 -ipo -x3 -no-prec-div -unroll2 -auto-ilp32  
-ansi-alias

---

Continued on next page
Cisco Systems
Cisco UCS C420 M3 (Intel Xeon E5-4607, 2.20 GHz)

<table>
<thead>
<tr>
<th>SPECint2006</th>
<th>33.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_base2006</td>
<td>31.4</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>peak Optimization Flags (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)</td>
</tr>
<tr>
<td>-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)</td>
</tr>
<tr>
<td>-unroll4</td>
</tr>
</tbody>
</table>

| 462.libquantum: basepeak = yes |
| 464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) |
| -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) |
| -unroll2 -ansi-alias |

Peak Other Flags

C benchmarks:

| 403.gcc: -Dalloca=_alloca |

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic13-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic13-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Originally published on 23 April 2013.