# Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

**SPEClnt\_rate2006 = 1090**

| SPECint\_rate\_base2006 = 1050 |

**CPU2006 license:** 9019

**Test sponsor:** Cisco Systems

**Tested by:** Cisco Systems

**Hardware**

- **CPU Name:** Intel Xeon E5-4640
- **CPU Characteristics:** Intel Turbo Boost Technology up to 2.80 GHz
- **CPU MHz:** 2400
- **FPU:** Integrated
- **CPU(s) enabled:** 32 cores, 4 chips, 8 cores/chip, 2 threads/core
- **CPU(s) orderable:** 1,2,3,4 chip
- **Primary Cache:** 32 KB I + 32 KB D on chip per core
- **Secondary Cache:** 256 KB I+D on chip per core
- **L3 Cache:** 20 MB I+D on chip per chip
- **Other Cache:** None
- **Memory:** 256 GB (32 x 8 GB 2Rx4 PC3-12800R-11, ECC)
- **Disk Subsystem:** 1 X 600GB SAS, 10K RPM
- **Other Hardware:** None

**Software**

- **Operating System:** Red Hat Enterprise Linux Server release 6.3 (Santiago) 2.6.32-279.el6.x86_64
- **Compiler:** C/C++: Version 12.1.3.293 of Intel C++ Studio XE for Linux
- **Auto Parallel:** No
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 32-bit
- **Peak Pointers:** 32/64-bit
- **Other Software:** Microquill SmartHeap V9.01
Cisco Systems
Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC CINT2006

SPECint_rate2006 = 1090
SPECint_rate_base2006 = 1050

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Base</td>
<td></td>
<td></td>
<td>Peak</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>400.perlbench</td>
<td>64</td>
<td>806</td>
<td>776</td>
<td>804</td>
<td>778</td>
<td>806</td>
<td>775</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>401.bzip2</td>
<td>64</td>
<td>1053</td>
<td>586</td>
<td>1053</td>
<td>587</td>
<td>1054</td>
<td>586</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>403.gcc</td>
<td>64</td>
<td>616</td>
<td>837</td>
<td>618</td>
<td>834</td>
<td>615</td>
<td>838</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>429.mcf</td>
<td>64</td>
<td>357</td>
<td>1640</td>
<td>355</td>
<td>1640</td>
<td>355</td>
<td>1640</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>445.gobmk</td>
<td>64</td>
<td>858</td>
<td>783</td>
<td>857</td>
<td>783</td>
<td>858</td>
<td>783</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>456.hmer</td>
<td>64</td>
<td>455</td>
<td>1320</td>
<td>451</td>
<td>1320</td>
<td>449</td>
<td>1330</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>458.sjeng</td>
<td>64</td>
<td>992</td>
<td>780</td>
<td>992</td>
<td>781</td>
<td>992</td>
<td>780</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>462.libquantum</td>
<td>64</td>
<td>210</td>
<td>6330</td>
<td>210</td>
<td>6320</td>
<td>210</td>
<td>6320</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>464.h264ref</td>
<td>64</td>
<td>1076</td>
<td>1320</td>
<td>1076</td>
<td>1330</td>
<td>1076</td>
<td>1320</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>471.onmnetpp</td>
<td>64</td>
<td>637</td>
<td>628</td>
<td>637</td>
<td>628</td>
<td>637</td>
<td>628</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>473.astar</td>
<td>64</td>
<td>729</td>
<td>616</td>
<td>727</td>
<td>618</td>
<td>727</td>
<td>618</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>64</td>
<td>407</td>
<td>1080</td>
<td>407</td>
<td>1090</td>
<td>407</td>
<td>1090</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Power Technology set to Custom
Processor Power State C6 set to Disabled
Processor Power State C1 Enhanced set to Disabled
Energy Performance Set to Performance
DRAM Clock Throttling Set to Performance

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6800
$Rev: 6800 $ $Date:: 2011-10-11 #$ 6f2ebdf5032aaa42e583f96b07f99d3
running on SPECCPU-RHEL6.3 Thu May 16 23:32:39 2013

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) CPU E5-4640 0 @ 2.40GHz

Continued on next page
Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

**SPECint_rate2006 =** 1090

**SPECint_rate_base2006 =** 1050

**CPU2006 license:** 9019

**Test sponsor:** Cisco Systems

**Test date:** May-2013

** Tested by:** Cisco Systems

**Hardware Availability:** Nov-2012

**Software Availability:** Dec-2011

---

### Platform Notes (Continued)

- 4 "physical id"s (chips)
- 64 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores : 8
  - siblings : 16
  - physical 0: cores 0 1 2 3 4 5 6 7
  - physical 1: cores 0 1 2 3 4 5 6 7
  - physical 2: cores 0 1 2 3 4 5 6 7
  - physical 3: cores 0 1 2 3 4 5 6 7
- cache size : 20480 KB

From /proc/meminfo

MemTotal: 264502612 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d

Red Hat Enterprise Linux Server release 6.3 (Santiago)

From /etc/*release* /etc/*version*

redhat-release: Red Hat Enterprise Linux Server release 6.3 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.3 (Santiago)

uname -a:

Linux SPECCPU-RHEL6.3 2.6.32-279.el6.x86_64 #1 SMP Wed Jun 13 18:24:36 EDT 2012 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 16 16:21

SPEC is set to: /opt/cpu2006-1.2

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 ext4 274G 9.4G 251G 4% /

Additional information from dmidecode:

Memory:

32x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 2 rank

(End of data from sysinfo program)

### General Notes

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64"

Binaries compiled on a system with 2 X Intel Xeon E5-2690 CPU + 128 GB memory using RHEL 6.2

Transparent Huge Pages enabled with:

echo always > /sys/kernel/mm/redhat_transparenthugepage/enabled

Continued on next page
Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

SPECint_rate2006 = 1090
SPECint_rate_base2006 = 1050

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
Test date: May-2013
Hardware Availability: Nov-2012
Software Availability: Dec-2011

General Notes (Continued)
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches

Base Compiler Invocation

C benchmarks:
  icc  -m32
C++ benchmarks:
  icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
  -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
C++ benchmarks:
  -xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
  -Wl,-z,muldefs -L/smartheap -lsmartheap

Base Other Flags

C benchmarks:
  403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
  icc  -m32
  400.perlbench: icc  -m64
  401.bzip2: icc  -m64

Continued on next page
Cisco Systems

Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

SPECint_rate2006 = 1090
SPECint_rate_base2006 = 1050

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2013
Hardware Availability: Nov-2012
Software Availability: Dec-2011

Peak Compiler Invocation (Continued)

456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div
429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
  -ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll2 -ansi-alias

Continued on next page
Cisco Systems
Cisco UCS C420 M3 (Intel Xeon E5-4640, 2.40 GHz)

SPECint_rate2006 = 1090
SPECint_rate_base2006 = 1050

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2013
Hardware Availability: Nov-2012
Software Availability: Dec-2011

Peak Optimization Flags (Continued)

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/smartheap -lsmartheap

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic12.1-official-linux64.20120425.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130607.xml

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Originally published on 7 June 2013.