Cisco Systems

Cisco UCS C220 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

SPECint_rate2006 = 900
SPECint_rate_base2006 = 871

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware

CPU Name: Intel Xeon E5-2690 v2
CPU Characteristics: Intel Turbo Boost Technology up to 3.60 GHz
CPU MHz: 3000
FPU: Integrated
CPU(s) enabled: 20 cores, 2 chips, 10 cores/chip, 2 threads/core
CPU(s) orderable: 1.2 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 25 MB I+D on chip per chip
Other Cache: None
Memory: 128 GB (16 x 8 GB 2Rx4 PC3-14900R-13, ECC)
Disk Subsystem: 1 X 300 GB 15000 RPM SAS
Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.4 (Santiago)
Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0
Cisco Systems
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CPU2006 license: 9019
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Results Table

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<td>306</td>
<td>901</td>
<td>306</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
BIOS Settings:
Intel HT Technology = Enabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State C1 Enhanced set to Disabled
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on SL1-IVB Fri Nov 8 00:51:02 2013

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
Continued on next page
Cisco Systems
Cisco UCS C220 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

SPECint_rate2006 = 900
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) CPU E5-2690 v2 @ 3.00GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
  cache size : 25600 KB

From /proc/meminfo
  MemTotal: 132123300 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
  Red Hat Enterprise Linux Server release 6.4 (Santiago)

From /etc/*release* /etc/*version*
  redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
  system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)

uname -a:
  Linux SL1-IVB 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Nov 8 00:48

SPEC is set to: /opt/cpu2006-1.2
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sdb1 ext4 275G 234G 27G 90% /

Additional information from dmidecode:
  BIOS Cisco Systems, Inc. C220M3.1.5.2.27.071120132232 07/11/2013
  Memory:
  16x 0xAD00 HMT31GR7EFR4C-RD 8 GB 1866 MHz 2 rank

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib64:/opt/cpu2006-1.2/lib64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB

Continued on next page
## Cisco Systems
Cisco UCS C220 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

<table>
<thead>
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<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

### General Notes (Continued)
- memory using RedHat EL 6.4
- Transparent Huge Pages enabled with:
  - `echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled`
- Filesystem page cache cleared with:
  - `echo 1>/proc/sys/vm/drop_caches`
- `runcp` command invoked through `numactl` i.e.:
  - `numactl --interleave=all runcp <etc>`

### Base Compiler Invocation
- C benchmarks:
  - `icc -m32`
- C++ benchmarks:
  - `icpc -m32`

### Base Portability Flags
- 400.perlbench: `-DSPEC_CPU_LINUX_IA32`
- 462.libquantum: `-DSPEC_CPU_LINUX`
- 483.xalancbmk: `-DSPEC_CPU_LINUX`

### Base Optimization Flags
- C benchmarks:
  - `-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3`
- C++ benchmarks:
  - `-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3`
  - `-Wl,-z,muldefs -L/sh -lsmartheap`

### Base Other Flags
- C benchmarks:
  - 403.gcc: `-Dalloca=_alloca`

### Peak Compiler Invocation
- C benchmarks (except as noted below):
  - `icc -m32`
Cisco Systems
Cisco UCS C220 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

SPECint_rate2006 = 900
SPECint_rate_base2006 = 871

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2013
Hardware Availability: Sep-2013
Software Availability: Sep-2013

Peak Compiler Invocation (Continued)

400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32
401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias
403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div
429.mcf: basepeak = yes
445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -ansi-alias -opt-mem-layout-trans=3
456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto-ilp32

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Cisco Systems
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2013
Hardware Availability: Sep-2013
Software Availability: Sep-2013

Peak Optimization Flags (Continued)

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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