Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

SPECint\_rate\_base2006 = 868

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Dec-2013
Hardware Availability: Dec-2013
Tested by: Cisco Systems
Software Availability: Sep-2013

<table>
<thead>
<tr>
<th>Program</th>
<th>Copies</th>
<th>Specint_rate2006</th>
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<tr>
<td>400.perlbench</td>
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<td>401.bzip2</td>
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<td>403.gcc</td>
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<td>429.mcf</td>
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<td>456.hmmer</td>
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<td>473.astar</td>
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<tr>
<td>483.xalancbmk</td>
<td>40</td>
<td>904</td>
<td></td>
</tr>
</tbody>
</table>

Hardware

CPU Name: Intel Xeon E5-2690 v2
CPU Characteristics: Intel Turbo Boost Technology up to 3.60 GHz
CPU MHz: 3000
FPU: Integrated
CPU(s) enabled: 20 cores, 2 chips, 10 cores/chip, 2 threads/core
CPU(s) orderable: 1.2 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: None
Other Cache: None
Memory: 128 GB (16 x 8 GB 2Rx4 PC3-14900R-13, ECC)
Disk Subsystem: 1 X 600 GB 10000 RPM SAS
Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.4 (Santiago)
Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0
Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
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RESULTS TABLE

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds Base</th>
<th>Ratio Base</th>
<th>Seconds Ratio</th>
<th>Seconds Peak</th>
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<td>793</td>
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<td>547</td>
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<tr>
<td>astar</td>
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<tr>
<td>salancmbk</td>
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<td>306</td>
<td>902</td>
<td>305</td>
<td>905</td>
<td>305</td>
</tr>
</tbody>
</table>

RESULTS APPEAR IN THE ORDER IN WHICH THEY WERE RUN. BOLD UNDERLINED TEXT INDICATES A MEDIAN MEASUREMENT.

SUBMIT NOTES
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

OPERATING SYSTEM NOTES
Stack size set to unlimited using "ulimit -s unlimited"

PLATFORM NOTES
BIOS Settings:
- Intel HT Technology = Enabled
- CPU performance set to HPC
- Power Technology set to Custom
- CPU Power State C6 set to Enabled
- CPU Power State C1 Enhanced set to Disabled
- Energy Performance policy set to Performance
- Memory RAS configuration set to Maximum Performance
- DRAM Clock Throttling Set to Performance
- LV DDR Mode set to Performance-mode
- DRAM Refresh Rate Set to 1x
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on localhost.localdomain Wed Dec 4 19:39:01 2013

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
Continued on next page
Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

**SPECint_rate2006 = 899**
**SPECint_rate_base2006 = 868**

<table>
<thead>
<tr>
<th>CPU2006 license:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
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<tr>
<td>Test date:</td>
<td>Dec-2013</td>
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<td>Dec-2013</td>
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<tr>
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<td>Sep-2013</td>
</tr>
</tbody>
</table>

---

**Platform Notes (Continued)**

http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

- **model name**: Intel(R) Xeon(R) CPU E5-2690 v2 @ 3.00GHz
- **2 "physical id"s (chips)**
- **40 "processors"**
- **cores, siblings**: (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - **cpu cores**: 10
  - **siblings**: 20
  - **physical 0: cores**: 0 1 2 3 4 8 9 10 11 12
  - **physical 1: cores**: 0 1 2 3 4 8 9 10 11 12
- **cache size**: 25600 KB

From /proc/meminfo

- **MemTotal**: 132086392 kB
- **HugePages_Total**: 0
- **Hugepagesize**: 2048 kB

/usr/bin/lsb_release -d

- Red Hat Enterprise Linux Server release 6.4 (Santiago)

From /etc/*release* /etc/*version*

- redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
- system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)

uname -a:

- Linux localhost.localdomain 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013 x86_64 x86_64 x86_64 GNU/Linux
- run-level 3 Dec 4 19:34

SPEC is set to: /opt/cpu2006-1.2

Filesystem | Type | Size | Used | Avail | Use% | Mounted on
---|---|---|---|---|---|---
/dev/sda1 | ext4 | 550G | 37G | 485G | 8% | /

Additional information from dmidecode:

- BIOS Cisco Systems, Inc. B200M3.2.1.3.a.0.082320131800 08/23/2013
- Memory:
  - 16x 0xAD00 HMT31GR7EFR4C-RD 8 GB 1866 MHz 2 rank
  - 8x NO DIMM NO DIMM

(End of data from sysinfo program)

---

**General Notes**

Environment variables set by runspec before the start of the run:

LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib32:/opt/cpu2006-1.2/lib64:/opt/cpu2006-1.2/sh"

Continued on next page
Cisco Systems
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General Notes (Continued)

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32
C++ benchmarks:
icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
C++ benchmarks:
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-stdc++fixes -Wl,-z,muldefs -L/sh -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32

Continued on next page
Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2690 v2, 3.00 GHz)

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Peak Compiler Invocation (Continued)

400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4 -auto-ilp32

Continued on next page
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Peak Optimization Flags (Continued)

462.libquantum: basepeak = yes
464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:
471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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