Cisco Systems
Cisco UCS B200 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>December 2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU License:</td>
<td>9019</td>
</tr>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
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<tr>
<td>Tested By:</td>
<td>Cisco Systems</td>
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</tbody>
</table>

**SPECint_rate2006 = 429**
**SPECint_rate_base2006 = 414**

### Hardware
- **CPU Name:** Intel Xeon E5-2620 v2
- **CPU Characteristics:** Intel Turbo Boost Technology up to 2.60 GHz
- **CPU MHz:** 2100
- **FPU:** Integrated
- **CPU(s) enabled:** 12 cores, 2 chips, 6 cores/chip, 2 threads/core
- **CPU(s) orderable:** 1.2 chip
- **Primary Cache:** 32 KB I + 32 KB D on chip per core
- **Secondary Cache:** 256 KB I+D on chip per core
- **L3 Cache:** 15 MB I+D on chip per chip
- **Other Cache:** None
- **Memory:** 256 GB (16 x 16 GB 2Rx4 PC3-14900R-13, ECC, running at 1600 MHz and CL7)
- **Disk Subsystem:** 1 X 300 GB 15000 RPM SAS
- **Other Hardware:** None

### Software
- **Operating System:** Red Hat Enterprise Linux Server release 6.4 (Santiago)
- **Compiler:** C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
- **Auto Parallel:** No
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 32-bit
- **Peak Pointers:** 32/64-bit
- **Other Software:** Microquill SmartHeap V10.0

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**Diagram of Test Results**
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>xalancbmk</td>
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<td>470</td>
<td>24</td>
<td>353</td>
<td>469</td>
<td>351</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
BIOS Settings:
Intel HT Technology = Enabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State C1 Enhanced set to Disabled
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on B200M3-IVB Wed Dec 4 19:42:07 2013

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
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CPU2006 license: 9019
Test sponsor: Cisco Systems
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Platform Notes (Continued)

http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2620 v2 @ 2.10GHz
  2 "physical id"s (chips)
  24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 6
siblings : 12
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
cache size : 15360 KB

From /proc/meminfo
MemTotal: 264462736 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)

From /etc/*release*/etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
uname -a:
Linux B200M3-IVB 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 4 19:39

SPEC is set to: /opt/cpu2006-1.2

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 275G 35G 226G 14% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. B200M3.2.1.3a.0.082320131800 08/23/2013
Memory:
16x 0xAD00 HMT42GR7AFR4C-RD 16 GB 1600 MHz 2 rank
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

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<td>Hardware Availability:</td>
<td>Dec-2013</td>
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<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Sep-2013</td>
</tr>
</tbody>
</table>

**General Notes (Continued)**

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

**Base Compiler Invocation**

C benchmarks:
-icc -m32

C++ benchmarks:
-icpc -m32

**Base Portability Flags**

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

**Base Optimization Flags**

C benchmarks:
-xxSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:
-xxSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/sh -lsmartheap

**Base Other Flags**

C benchmarks:
403.gcc: -Dalloca=_alloca

**Peak Compiler Invocation**

C benchmarks (except as noted below):
-icc -m32

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Peak Compiler Invocation (Continued)

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<td>400.perlbench</td>
<td>icc -m64</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>icc -m64</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>icc -m64</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>icc -m64</td>
</tr>
<tr>
<td>C++ benchmarks:</td>
<td>icpc -m32</td>
</tr>
</tbody>
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Peak Portability Flags

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<tr>
<td>400.perlbench</td>
<td>-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>-DSPEC_CPU_LP64</td>
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<tr>
<td>462.libquantum</td>
<td>-DSPEC_CPU_LINUX</td>
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<td>483.xalancbmk</td>
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Peak Optimization Flags

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<td>400.perlbench</td>
<td>-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias</td>
</tr>
<tr>
<td>403.gcc</td>
<td>-xSSE4.2 -ipo -O3 -no-prec-div</td>
</tr>
<tr>
<td>429.mcf</td>
<td>basepeak = yes</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>-xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -ansi-alias -opt-mem-layout-trans=3</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>-xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>-xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto-ilp32</td>
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Peak Optimization Flags (Continued)

462.libquantum: basepeak = yes
464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:
471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes
483.xalanbmk: basepeak = yes

Peak Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml

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