Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2670 v2, 2.50 GHz)

<table>
<thead>
<tr>
<th>SPECfp_rate_base2006</th>
<th>606</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECfp_rate2006</td>
<td>620</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System: Red Hat Enterprise Linux Server release 6.4 (Santiago) 2.6.32-358.el6.x86_64</td>
<td>CPU Name: Intel Xeon E5-2670 v2</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux; Fortran: Version 14.0.0.080 of Intel Fortran Studio XE for Linux</td>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 3.30 GHz</td>
</tr>
<tr>
<td>Auto Parallel: No</td>
<td>CPU MHz: 2500</td>
</tr>
<tr>
<td>File System: ext4</td>
<td>FPU: Integrated</td>
</tr>
<tr>
<td></td>
<td>CPU(s) enabled: 20 cores, 2 chips, 10 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td></td>
<td>CPU(s) orderable: 1,2 chip</td>
</tr>
<tr>
<td></td>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td></td>
<td>Secondary Cache: 256 KB I+D on chip per core</td>
</tr>
</tbody>
</table>

Test date: Dec-2013
Hardware Availability: Dec-2013
Software Availability: Sep-2013

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECfp_rate2006</th>
<th>SPECfp_rate_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>40</td>
<td>503</td>
</tr>
<tr>
<td>416.gamess</td>
<td>40</td>
<td>657</td>
</tr>
<tr>
<td>433.milc</td>
<td>40</td>
<td>478</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>40</td>
<td>478</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>40</td>
<td>689</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>40</td>
<td>813</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>20</td>
<td>364</td>
</tr>
<tr>
<td>444.namd</td>
<td>40</td>
<td>337</td>
</tr>
<tr>
<td>447.dealII</td>
<td>40</td>
<td>511</td>
</tr>
<tr>
<td>450.soplex</td>
<td>20</td>
<td>406</td>
</tr>
<tr>
<td>453.povray</td>
<td>40</td>
<td>355</td>
</tr>
<tr>
<td>454.calculix</td>
<td>40</td>
<td>887</td>
</tr>
<tr>
<td>459.GemsFD</td>
<td>40</td>
<td>319</td>
</tr>
<tr>
<td>465.tonto</td>
<td>40</td>
<td>716</td>
</tr>
<tr>
<td>470.lbm</td>
<td>40</td>
<td>635</td>
</tr>
<tr>
<td>481.wrf</td>
<td>40</td>
<td>596</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>40</td>
<td>594</td>
</tr>
</tbody>
</table>

Continued on next page
Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2670 v2, 2.50 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

L3 Cache: 25 MB I+D on chip per chip
Other Cache: None
Memory: 128 GB (16 x 8 GB 2Rx4 PC3-14900R-13, ECC)
Disk Subsystem: 1 X 300 GB 15000 RPM SAS
Other Hardware: None

System State: Run level 3 (multi-user)
Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: None

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base Seconds</th>
<th>Ratio</th>
<th>Base Seconds</th>
<th>Ratio</th>
<th>Peak Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>40</td>
<td>1081</td>
<td>503</td>
<td>1081</td>
<td>503</td>
<td>1080</td>
<td>503</td>
<td>40</td>
<td>1081</td>
<td>503</td>
<td>1080</td>
<td>503</td>
</tr>
<tr>
<td>416.gamess</td>
<td>40</td>
<td>1210</td>
<td>647</td>
<td>1211</td>
<td>647</td>
<td>1210</td>
<td>647</td>
<td>40</td>
<td>1192</td>
<td>657</td>
<td>1191</td>
<td>657</td>
</tr>
<tr>
<td>433.milc</td>
<td>40</td>
<td>769</td>
<td>478</td>
<td>769</td>
<td>477</td>
<td>769</td>
<td>478</td>
<td>40</td>
<td>769</td>
<td>478</td>
<td>769</td>
<td>478</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>40</td>
<td>528</td>
<td>689</td>
<td>527</td>
<td>690</td>
<td>528</td>
<td>689</td>
<td>40</td>
<td>528</td>
<td>689</td>
<td>527</td>
<td>690</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>40</td>
<td>354</td>
<td>808</td>
<td>357</td>
<td>800</td>
<td>357</td>
<td>800</td>
<td>40</td>
<td>351</td>
<td>813</td>
<td>353</td>
<td>808</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>40</td>
<td>620</td>
<td>771</td>
<td>619</td>
<td>772</td>
<td>622</td>
<td>769</td>
<td>40</td>
<td>620</td>
<td>771</td>
<td>619</td>
<td>772</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>40</td>
<td>1115</td>
<td>337</td>
<td>1114</td>
<td>337</td>
<td>1113</td>
<td>338</td>
<td>20</td>
<td>516</td>
<td>364</td>
<td>515</td>
<td>365</td>
</tr>
<tr>
<td>444.namd</td>
<td>40</td>
<td>643</td>
<td>499</td>
<td>630</td>
<td>509</td>
<td>630</td>
<td>509</td>
<td>40</td>
<td>635</td>
<td>505</td>
<td>628</td>
<td>511</td>
</tr>
<tr>
<td>447.dealII</td>
<td>40</td>
<td>409</td>
<td>1120</td>
<td>409</td>
<td>1120</td>
<td>407</td>
<td>1120</td>
<td>40</td>
<td>409</td>
<td>1120</td>
<td>409</td>
<td>1120</td>
</tr>
<tr>
<td>450.soplex</td>
<td>40</td>
<td>942</td>
<td>354</td>
<td>940</td>
<td>355</td>
<td>940</td>
<td>355</td>
<td>20</td>
<td>411</td>
<td>406</td>
<td>411</td>
<td>406</td>
</tr>
<tr>
<td>453.povray</td>
<td>40</td>
<td>240</td>
<td>887</td>
<td>240</td>
<td>886</td>
<td>239</td>
<td>892</td>
<td>40</td>
<td>205</td>
<td>1040</td>
<td>208</td>
<td>1020</td>
</tr>
<tr>
<td>454.calculix</td>
<td>40</td>
<td>338</td>
<td>976</td>
<td>338</td>
<td>977</td>
<td>338</td>
<td>977</td>
<td>40</td>
<td>338</td>
<td>976</td>
<td>338</td>
<td>977</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>40</td>
<td>1334</td>
<td>318</td>
<td>1330</td>
<td>319</td>
<td>1332</td>
<td>319</td>
<td>40</td>
<td>1334</td>
<td>318</td>
<td>1330</td>
<td>319</td>
</tr>
<tr>
<td>465.tonto</td>
<td>40</td>
<td>574</td>
<td>686</td>
<td>572</td>
<td>688</td>
<td>577</td>
<td>682</td>
<td>40</td>
<td>552</td>
<td>713</td>
<td>550</td>
<td>716</td>
</tr>
<tr>
<td>470.lbm</td>
<td>40</td>
<td>865</td>
<td>635</td>
<td>866</td>
<td>635</td>
<td>866</td>
<td>635</td>
<td>40</td>
<td>865</td>
<td>635</td>
<td>866</td>
<td>635</td>
</tr>
<tr>
<td>481.wrf</td>
<td>40</td>
<td>750</td>
<td>596</td>
<td>757</td>
<td>590</td>
<td>750</td>
<td>596</td>
<td>40</td>
<td>750</td>
<td>596</td>
<td>750</td>
<td>596</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>40</td>
<td>1254</td>
<td>622</td>
<td>1257</td>
<td>620</td>
<td>1258</td>
<td>620</td>
<td>40</td>
<td>1317</td>
<td>592</td>
<td>1313</td>
<td>594</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HT Technology = Enabled
CPU performance set to HPC

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Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2670 v2, 2.50 GHz)

**SPEC CFP2006 Result**

<table>
<thead>
<tr>
<th>SPECfp_rate2006</th>
<th>SPECfp_rate_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>620</td>
<td>606</td>
</tr>
</tbody>
</table>

**CPU2006 license:** 9019
**Test date:** Dec-2013
**Test sponsor:** Cisco Systems
**Tested by:** Cisco Systems
**Hardware Availability:** Dec-2013
**Software Availability:** Sep-2013

### Platform Notes (Continued)

Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State C1 Enhanced set to Disabled
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on C240M3-ivb Sun Dec 22 15:11:17 2013

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2670 v2 @ 2.50GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12
  cache size : 25600 KB
From /proc/meminfo
MemTotal:       132123164 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)

uname -a:
Linux C240M3-ivb 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 22 15:00

SPEC is set to: /opt/cpu2006-1.2

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda1</td>
<td>ext4</td>
<td>275G</td>
<td>13G</td>
<td>248G</td>
<td>5%</td>
<td>/</td>
</tr>
</tbody>
</table>

Continued on next page
Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2670 v2, 2.50 GHz)

SPECfp_rate2006 = 620
SPECfp_rate_base2006 = 606

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Additional information from dmidecode:
BIOS Cisco Systems, Inc. C240M3.1.5.3b.0.082020130616 08/20/2013
Memory: 16x 0xAD00 HMT31GR7EFR4C-RD 8 GB 1866 MHz 2 rank
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
  icc  -m64
C++ benchmarks:
  icpc  -m64
Fortran benchmarks:
  ifort  -m64
Benchmarks using both Fortran and C:
  icc  -m64 ifort  -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.reusmp: -DSPEC_CPU_LP64 -nofor_main
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64

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Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2670 v2, 2.50 GHz)

SPECfp_rate2006 = 620
SPECfp_rate_base2006 = 606

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2013
Hardware Availability: Dec-2013
Software Availability: Sep-2013

Base Portability Flags (Continued)

447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.libm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

C++ benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Fortran benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch

Benchmarks using both Fortran and C:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64

482.sphinx3: icc -m32

C++ benchmarks (except as noted below):
icpc -m64

450.soplex: icpc -m32

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64
Cisco Systems
Cisco UCS C240 M3 (Intel Xeon E5-2670 v2, 2.50 GHz)

| SPECfp_rate2006 = | 620 |
| SPECfp_rate_base2006 = | 606 |

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>416.gamess</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>433.milc</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>-DSPEC_CPU_LP64 -nofor_main</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>-DSPEC_CPU_LP64 -nofor_main</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>444.namd</td>
<td>-DSPEC_CPU_LP64 -nofor_main</td>
</tr>
<tr>
<td>447.dealII</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>453.povray</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>454.calculix</td>
<td>-DSPEC_CPU_LP64 -nofor_main</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>465.tonto</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>470.lbm</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>481.wrf</td>
<td>-DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX</td>
</tr>
</tbody>
</table>

Peak Optimization Flags

C benchmarks:

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>433.milc</td>
<td>-xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2) -prof-use(pass 2) -auto-ilp32</td>
</tr>
<tr>
<td>470.lbm</td>
<td>basepeak = yes</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>-xAVX -ipo -O3 -no-prec-div -opt-mem-layout-trans=3 -unroll2</td>
</tr>
</tbody>
</table>

C++ benchmarks:

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>444.namd</td>
<td>-xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2) -prof-use(pass 2) -fno-alias -auto-ilp32</td>
</tr>
<tr>
<td>447.dealII</td>
<td>basepeak = yes</td>
</tr>
<tr>
<td>450.soplex</td>
<td>-xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2) -prof-use(pass 2) -opt-malloc-options=3</td>
</tr>
<tr>
<td>453.povray</td>
<td>-xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2) -prof-use(pass 2) -unroll4 -ansi-alias</td>
</tr>
</tbody>
</table>

Fortran benchmarks:

Continued on next page
Peak Optimization Flags (Continued)

410.bwaves: basepeak = yes
416.gamess: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
   -no-prec-div(pass 2) -prof-use(pass 2) -unroll2
   -inline-level=0 -scalar-rep-
434.zeusmp: basepeak = yes
437.leslie3d: -xAVX -ipo -O3 -no-prec-div -opt-prefetch
459.GemsFDTD: basepeak = yes
465.tonto: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
   -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto
   -inline-calloc -opt-malloc-options=3

Benchmarks using both Fortran and C:

435.gromacs: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
   -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
   -prof-use(pass 2) -opt-prefetch -auto-ilp32
436.cactusADM: basepeak = yes
454.calculix: basepeak = yes
481.wrf: -xAVX -ipo -O3 -no-prec-div -auto-ilp32

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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