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<table>
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<th>Description</th>
</tr>
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</tr>
<tr>
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<td>473.astar</td>
<td></td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td></td>
</tr>
</tbody>
</table>

**Hardware**
- **CPU Name:** Intel Xeon E7-4830 v2
- **CPU Characteristics:** Intel Turbo Boost Technology up to 2.70 GHz
- **CPU MHz:** 2200
- **CPU:** Integrated
- **CPU(s) enabled:** 20 cores, 2 chips, 10 cores/chip, 2 threads/core
- **Primary Cache:** 32 KB I + 32 KB D on chip per core
- **Secondary Cache:** 256 KB I+D on chip per core
- **L3 Cache:** 20 MB I+D on chip per chip
- **Other Cache:** None

**Software**
- **Operating System:** Red Hat Enterprise Linux Server release 6.5 (Santiago) 2.6.32-431.el6.x86_64
- **Compiler:** C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
- **Auto Parallel:** Yes
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 32/64-bit
- **Peak Pointers:** 32/64-bit

Non-Compliant
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Platform Notes**

Intel HT Technology = Enabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Disabled
CPU Power State C1 Enhanced set to Disabled
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance

$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>Peak</th>
</tr>
</thead>
<tbody>
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<td>Seconds</td>
<td>Ratio</td>
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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.
SPEC CINT2006 Result

Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4830 v2, 2.20 GHz)

SPECint2006 = NC
SPECint_base2006 = NC

CPU2006 license: 9019
Test date: Apr-2014
Test sponsor: Cisco Systems
Hardware Availability: May-2014
Tested by: Cisco Systems
Software Availability: Sep-2013

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Platform Notes (Continued)

running on yos Sun Apr 20 11:09:39 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E7-4830 v2 @ 2.20GHz
2 "physical id"s (chips)
40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
cache size : 20480 KB

From /proc/meminfo
MemTotal:       263970536 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.5 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
uname -a:
Linux yos 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54 EST 2013 x86_64
x86_64 x86_64 GNU/Linux
run-level 3 Apr 20 11:07

SPEC is set to: /opt/cpu2006-1.4

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 275G 48G 213G 19% /

Continued on next page
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Platform Notes (Continued)

Additional information from dmidecode:
BIOS Cisco Systems, Inc. EXM4-1.2.2.1.15.1.0 2020-1613 02/20/2014
Memory:
32x 8 GB
32x 0xCE00 M393B1K70QB0-YK0 8 GB 1333 MHz 2 rank
16x NO DIMM NO DIMM
(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/opt/cpu2006-1.4/libs/32:/opt/cpu2006-1.4/libs/64:/opt/cpu2006-1.4/sh"
OMP_NUM_THREADS = "40"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
runspec command --noexecve through numactl i.e.:
umactl --interleave=all runspec <etc>

Base Compiler Invocation

icc -m64
C++ benchmarks:
icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64

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**Base Portability Flags (Continued)**

- 401.bzip2: -DSPEC_CPU_LP64
- 403.gcc: -DSPEC_CPU_LP64
- 429.mcf: -DSPEC_CPU_LP64
- 445.gobmk: -DSPEC_CPU_LP64
- 456.hmmer: -DSPEC_CPU_LP64
- 458.sjeng: -DSPEC_CPU_LP64
- 462.libquantum: -DSPEC_CPU_LP64, -DSPEC_CPU_LINUX
- 464.h264ref: -DSPEC_CPU_LP64
- 471.omnetpp: -DSPEC_CPU_LP64
- 473.astar: -DSPEC_CPU_LP64
- 483.xalancbmk: -DSPEC_CPU_LINUX, -DSPEC_CPU_LP64

**Base Optimization Flags**

C benchmarks:
- xsse4.2 -ipo -no-prec-div -parallel -opt-prefetch -auto-p32

C++ benchmarks:
- xsse4.2 -ipo -O2 no-prec-div -opt-prefetch -auto-p32
- Wl,-z,muldefs -L/sh -lsmartheap64

**Base Other Flags**

- 403.gcc: -Dalloca=_alloca

**Peak Compiler Invocation**

C benchmarks (except as noted below):
- icc -m64

400.perlbench: icc -m32

Continued on next page
Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4830 v2, 2.20 GHz)

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Peak Compiler Invocation (Continued)

445.gobmk: icc -m32
464.h264ref: icc -m32

C++ benchmarks (except as noted below):
icpc -m32
473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX=
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -SPEC_CPU_LINUX

Peak Optimization Flags

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -ansi-alias

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32
-opt-prefetch -ansi-alias

403.gcc: -xSSE4.2 -ipo -O3 -no-prec-div -inline-calloc
-opt-malloc-options=3 -auto-ilp32

Continued on next page
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Peak Optimization Flags (Continued)

429.mcf: basepeak = yes
445.gobmk: -xsse4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
          -ansi-alias
456.hmmer: -xsse4.2 -ipo -o3 -no-prec-div -unroll2 -auto-ilp32
          -ansi-alias
458.sjeng: -xsse4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
          -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
          -unroll4
462.libquantum: basepeak = yes
464.h264ref: -xsse4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
          -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
          -unroll4 -ansi-alias

C++ benchmarks:
471.omnetpp: -xsse4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
          -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
          -opt-ra-region-strategy=block -ansi-alias
          -Wl,-z,muldefs -L/sh -lsmartheap
473.astar: basepeak = yes
492.abc: -xsse4.2 -ipo -o3 -no-prec-div -opt-prefetch -ansi-alias
          -Wl,-z,muldefs -L/sh -lsmartheap

Peak Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

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The flags files that were used to format this result can be browsed at:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20140311.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20140311.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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Non-Compliant