Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4850 v2, 2.30 GHz)

<table>
<thead>
<tr>
<th>SPECfp_rate2006</th>
<th>SPECfp_rate_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
Test date: Apr-2014
Hardware Availability: May-2014
Software Availability: Sep-2013

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

<table>
<thead>
<tr>
<th>Copies</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
</tr>
<tr>
<td>416.gamess</td>
</tr>
<tr>
<td>433.milc</td>
</tr>
<tr>
<td>434.zeusmp</td>
</tr>
<tr>
<td>435.gromacs</td>
</tr>
<tr>
<td>436.cactusADM</td>
</tr>
<tr>
<td>437.leslie3d</td>
</tr>
<tr>
<td>444.namd</td>
</tr>
<tr>
<td>447.dealII</td>
</tr>
<tr>
<td>450.soplex</td>
</tr>
<tr>
<td>453.povray</td>
</tr>
<tr>
<td>454.calculix</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
</tr>
<tr>
<td>465.tonto</td>
</tr>
<tr>
<td>470.lbm</td>
</tr>
<tr>
<td>481.wrf</td>
</tr>
<tr>
<td>482.sphinx3</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4850 v2, 2.30 GHz)

SPECfp_rate2006 = NC
SPECfp_rate_base2006 = NC

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Apr-2014
Hardware Availability: May-2014
Software Availability: Sep-2013

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon E7-4850 v2</td>
<td>Operating System: Red Hat Enterprise Linux Server release 6.4 (Santiago)</td>
</tr>
<tr>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 2.80 GHz</td>
<td>Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux; Fortran: Version 14.0.0.080 of Intel Fortran Studio XE for Linux</td>
</tr>
<tr>
<td>CPU MHz: 2300</td>
<td>Auto Parallel: No</td>
</tr>
<tr>
<td>FPU: Integrated</td>
<td>File System: ext4</td>
</tr>
<tr>
<td>CPU(s) enabled: 24 cores, 2 chips, 12 cores/chip, 2 threads/core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>CPU(s) orderable: 1.2 chip</td>
<td>Base Pointers: 32/64-bit</td>
</tr>
<tr>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
<td>Peak Pointers: 32/64-bit</td>
</tr>
<tr>
<td>Secondary Cache: 256 KB I+D on chip per core</td>
<td>Other Software: None</td>
</tr>
<tr>
<td>L3 Cache: 24 MB I+D on chip per chip</td>
<td></td>
</tr>
<tr>
<td>Other Cache: None</td>
<td></td>
</tr>
<tr>
<td>Memory: 256 GB (32 x 8 GB 2Rx4 PC3L-12800R-11, ECC)</td>
<td></td>
</tr>
<tr>
<td>Disk Subsystem: 1 X 300 GB 15000 RPM SAS</td>
<td></td>
</tr>
<tr>
<td>Other Hardware: None</td>
<td></td>
</tr>
</tbody>
</table>
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Results Table:

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>416.gameess</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>433.milc</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>24</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>24</td>
<td>NC</td>
</tr>
<tr>
<td>444.namd</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>447.dealII</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>450.soplex</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>24</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>24</td>
<td>NC</td>
</tr>
<tr>
<td>453.povray</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>454.calculix</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>465.tonto</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>470.lbm</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>481.wrf</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>48</td>
<td>NC</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4850 v2, 2.30 GHz)

SPECfps_rate2006 = NC
SPECfps_rate_base2006 = NC

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Platform Notes

Intel HT Technology = Enabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Disabled
CPU Power State C1 Enhanced set to Disable
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
Sysinfo program /opt/cpu2006-1.4/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on specompcpu Fri Apr 18 15:55:36 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E7-4850 v2 @ 2.30GHz
  2 "physical ids" (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13
cache size : 24576 KB

Meminfo
MemTotal: 264103304 kB
MemFree: 123675064 kB
Buffers: 14743464 kB
Cached: 13213456 kB

From /proc/meminfo
MemTotal: 264103304 kB
MemFree: 123675064 kB
Buffers: 14743464 kB
Cached: 13213456 kB

PagePages_Total: 0

Hardware Availability: May-2014
Software Availability: Sep-2013

Test sponsor: Cisco Systems
Tested by: Cisco Systems
CPU2006 license: 9019
Test date: Apr-2014
Continued on next page
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Platform Notes (Continued)

```
uname -a:
    Linux specompcpu 2.6.32-358.el6.x86_64 #1 SMP Mon Jan 29 11:47:41 EST 2013
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Apr 18 01:57

SPEC is set to: /opt/cpu2006-1.4
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1   ext4    275G   29G  232G  11% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. X54-1.2.2.1.12.012920142034 01/29/2014
Memory:
  32x   8 GB
  32x 0xCE00 M393B1K70QB0-YK0 8 GB 1333 MHz 2 rank
  16x NO DIMM NO DIMM

(End of data from sysinfo program)
```

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.4/libs/32:/opt/cpu2006-1.4/libs/64:/opt/cpu2006-1.4/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using Redhat EL 6.4
Transparent Huge Pages enabled with:
    echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
    echo 1 > /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
    numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
    icc  -m64

Non-Compliant
SPEC CFP2006 Result

Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4850 v2, 2.30 GHz)

SPECfp_rate2006 = NC
SPECfp_rate_base2006 = NC

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Continued on next page
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Base Optimization Flags (Continued)

C++ benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Fortran benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch

Benchmarks using both Fortran and C:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64
482.sphinx3: icc -m32
C++ benchmarks (except as noted below):
icpc -m64
450.soplex: icpc -m32
Fortran benchmarks:
ifort -m64
Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Peak Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64

Continued on next page
Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4850 v2, 2.30 GHz)

<table>
<thead>
<tr>
<th>CPU2006 license</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

Test date: Apr-2014
Hardware Availability: May-2014
Software Availability: Sep-2013

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

### Peak Portability Flags (Continued)

<table>
<thead>
<tr>
<th>Benchmark Name</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>435.gromacs</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>-DSPEC_CPU_LP64, -nofor_main</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>444.namd</td>
<td>-DSPEC_CPU_LP64, -nofor_main</td>
</tr>
<tr>
<td>447.dealII</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>453.povray</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>454.calculix</td>
<td>-DSPEC_CPU_LP64, -nofor_main</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>465.tonto</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>470.lbm</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>481.wrf</td>
<td>-DSPEC_CPU_LP64, -DSPEC_CPU_CASE_FLAG, -DSPEC_CPU_LINUX</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags

C benchmarks:

- **433.milc**
  - -xAVX (pass 2)
  - -prof-gen (pass 1)
  - -ipo (pass 2)
  - -O3 (pass 2)
  - -no-prec-div (pass 2)
  - -opt-mem-layout-trans=3 (pass 2)
  - -prof-use (pass 2)
  - -auto-ilp32

- **470.lbm**
  - basepeak = yes

- **482.sphinx3**
  - -xAVX
  - -ipo
  - -O3
  - -no-prec-div
  - -opt-mem-layout-trans=3
  - -unroll2

C++ benchmarks:

- **444.namd**
  - -xAVX (pass 2)
  - -prof-gen (pass 1)
  - -ipo (pass 2)
  - -O3 (pass 2)
  - -no-prec-div (pass 2)
  - -opt-mem-layout-trans=3 (pass 2)
  - -prof-use (pass 2)
  - -auto-ilp32

- **447.dealII**
  - basepeak = yes

- **450.soplex**
  - -xAVX (pass 2)
  - -prof-gen (pass 1)
  - -ipo (pass 2)
  - -O3 (pass 2)
  - -no-prec-div (pass 2)
  - -opt-mem-layout-trans=3 (pass 2)
  - -prof-use (pass 2)
  - -auto-ilp32

- **453.povray**
  - -xAVX (pass 2)
  - -prof-gen (pass 1)
  - -ipo (pass 2)
  - -O3 (pass 2)
  - -no-prec-div (pass 2)
  - -opt-mem-layout-trans=3 (pass 2)
  - -prof-use (pass 2)
  - -opt-malloc-options=3

Continued on next page
Cisco Systems
Cisco UCS B260 M4 (Intel Xeon E7-4850 v2, 2.30 GHz)

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Peak Optimization Flags (Continued)

453.povray: -xAVX(pass 2) -prof-gen(pass 1) -ipso(pass 2) -O3(pass 2)
-ano-pre-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:

410.bwaves: basepeak = yes
416.gamess: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-ano-pre-div(pass 2) -prof-use(pass 2) -unroll2
-inline-level=3 -scalar-reg-

434.zeusmp: basepeak = yes
437.leslie3d: -xAVX -ipo -O3 -no-pre-div -opt-prefetch

459.GemsFDTD: basepeak = yes
465.tonto: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-ano-pre-div(pass 2) -prof-use(pass 2) -unroll4 -auto
-inline-level=3 -scalar-alloc -opt-malloc-options=3

Benchmarks using both Fortran and C:

435.gromacs: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-ano-pre-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -opt-prefetch -auto-ilp32

454.calculix: basepeak = yes
481.wrf: -xAVX -ipo -O3 -no-pre-div -auto-ilp32

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20140311.html

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Apr-2014
Hardware Availability: May-2014
Software Availability: Sep-2013

Non-Compliant
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.