Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4830 v2 @ 2.20GHz)

| SPECint\_rate2006 = NC |
| SPECint\_rate\_base2006 = NC |

**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

**Software**
- **Operating System:** Red Hat Enterprise Linux Server release 6.4 (Santiago)  
- **Compiler:** C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux  
- **Auto Parallel:** No  
- **File System:** ext4  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 32-bit  
- **Peak Pointers:** 32/64-bit

**Hardware**
- **CPU Name:** Intel Xeon E7-4830 v2  
- **CPU Characteristics:** Intel Turbo Boost Technology up to 2.70 GHz  
- **CPU MHz:** 2200  
- **FPU:** Integrated  
- **CPU(s) enabled:** 40 cores, 4 chips, 10 cores/chip, 2 threads/core  
- **CPU(s) orderable:** 1,2,3,4 Chips  
- **Primary Cache:** 32 KB I + 32 KB D on chip per core  
- **Secondary Cache:** 256 KB I+D on chip per core  
- **L3 Cache:** 20 MB I+D on chip per chip  
- **Other Cache:** None

**Non-Compliant**
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.
SPEC CINT2006 Result

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Results Table

- Results appear in the order in which they were run. Bold underlined text indicates a median measurement.
- Submit Notes
  - The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.
- Operating System Notes
  - Stack size set to unlimited using "ulimit -s unlimited"
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CPU performance set to Enterprise
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State C1 Enhanced set to Disabled
Package C State Limit set to C0/C1 State
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on msc-sbrhel Sat Apr 19 09:01:56 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) CPU E7-4830 v2 @ 2.20GHz
4 "physical id"s (chips)
80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
physical 2: cores 0 1 2 3 4 8 9 10 11 12
physical 3: cores 0 1 2 3 4 8 9 10 11 12
cache size : 20480 KB

From /proc/meminfo

MemTotal: 529139556 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)

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Platform Notes (Continued)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)

uname -a:
Linux msc-sbrhel 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Apr 19 08:47

SPEC is set to: /opt/cpu2006-1.2
Filesystem    Type    Size  Used Avail Use% Mounted on
/dev/sda1     ext4    275G   13G  249G   5% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. C460M4.1.5.5.13.012720142211 01/27/2014
Memory:
64x   8 GB
64x 0xCE00 M393B1K70QB0-YK0 8 GB 1333 MHz 2 rank
32x NO DIMM NO DIMM
(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
export LD_LIBRARY_PATH="/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enable
Filesystem page cache cleared with:
echo 1 >> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

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<th>Base Compiler Invocation</th>
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<tbody>
<tr>
<td>C benchmarks:</td>
</tr>
<tr>
<td>icc -m32</td>
</tr>
<tr>
<td>C++ benchmarks:</td>
</tr>
<tr>
<td>icpc -m32</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Base Portability Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench:</td>
</tr>
<tr>
<td>-DSPEC_CPU_LINUX_IA32</td>
</tr>
<tr>
<td>462.libquantum:</td>
</tr>
<tr>
<td>-DSPEC_CPU_LINUX</td>
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<tr>
<td>483.xalancbmk:</td>
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<tr>
<td>-DSPEC_CPU_LINUX</td>
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<tr>
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<tr>
<td>-xSSE4.2 -ipo -no-prec-div -opt-prefetch -opt-mem-layout-trans=3</td>
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<tr>
<td>C++ benchmarks:</td>
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<tr>
<td>-xSSE4.2 -ipo -m32 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3</td>
</tr>
<tr>
<td>-Wall,-z,ndefs -I/sh -lsmartheap</td>
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</table>

<table>
<thead>
<tr>
<th>Base Other Flags</th>
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</thead>
<tbody>
<tr>
<td>C benchmarks:</td>
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<tr>
<td>403.gcc: -Dalloca=_alloca</td>
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</table>

<table>
<thead>
<tr>
<th>Peak Compiler Invocation</th>
</tr>
</thead>
<tbody>
<tr>
<td>C benchmarks (except as noted below):</td>
</tr>
<tr>
<td>icc -m32</td>
</tr>
</tbody>
</table>

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### Peak Compiler Invocation (Continued)

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<th>Benchmark</th>
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<tr>
<td>400.perlbench</td>
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<tr>
<td>401.bzip2</td>
<td><code>icc -m64</code></td>
</tr>
<tr>
<td>456.hmmer</td>
<td><code>icc -m64</code></td>
</tr>
<tr>
<td>458.sjeng</td>
<td><code>icc -m64</code></td>
</tr>
</tbody>
</table>

**C++ benchmarks:**

- `icpc -m32`

### Peak Portability Flags

- `400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
- `401.bzip2: -DSPEC_CPU_LP64`
- `456.hmmer: -DSPEC_CPU_LP64`
- `458.sjeng: -DSPEC_CPU_LP64`
- `462.libquantum: -DSPEC_CPU_LINUX`
- `483.xalancbmk: -DSPEC_CPU_LINUX`

### Peak Optimization Flags

**C benchmarks:**

- `400.perlbench: -O3 -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32`
- `401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias`
- `403.gcc: -xSSE4.2 -ipo -o3 -no-prec-div`
- `429.mcf: basepeak = yes`
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Peak Optimization Flags (Continued)

445.gobmk: -xSSE4.2 (pass 2) -prof-gen (pass 1) -prof-use (pass 2)
        -ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -o3 -no-prelax -unroll12 -auto-ilp32

458.sjeng: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2)
        -o3 (pass 2) -no-prelax -v (pass 2) -prof-use (pass 2)
        -unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2)
        -o3 (pass 2) -no-prelax -div (pass 2) -prof-use (pass 2)
        -unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2 (pass 2) -prof-gen (pass 1) -ipo (pass 2)
        -o3 (pass 2) -no-prelax -div (pass 2) -prof-use (pass 2)
        -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
        -l/sh = mathcheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

433.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20140311.html
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SPEC CINT2006 Result

SPECint_rate2006 = NO
SPECint_rate_base2006 = NO

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Apr-2014
Hardware Availability: Apr-2014
Software Availability: Sep-2013

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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20140311.xml

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For other inquiries, please contact webmaster@spec.org.

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