Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

SPEC fp_rate2006 = NC
SPEC fp_rate_base2006 = NC

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2014
Hardware Availability: Apr-2014
Software Availability: Sep-2013

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon E7-4809 v2</td>
<td>Operating System: Red Hat Enterprise Linux Server release 6.4 (Santiago)</td>
</tr>
<tr>
<td>CPU Characteristics:</td>
<td>Compiler:</td>
</tr>
<tr>
<td>CPU MHz: 1900</td>
<td>C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux;</td>
</tr>
<tr>
<td>FPU: Integrated</td>
<td>Fortran: Version 14.0.0.080 of Intel Fortran Studio XE for Linux</td>
</tr>
<tr>
<td>CPU(s) enabled: 24 cores, 4 chips, 6 cores/chip, 2 threads/core</td>
<td>Auto Parallel: No</td>
</tr>
<tr>
<td>CPU(s) orderable: 1,2,3,4 Chips</td>
<td>File System: ext4</td>
</tr>
<tr>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Secondary Cache: 256 KB I+D on chip per core</td>
<td>Base Pointers: 32/64-bit</td>
</tr>
<tr>
<td>L3 Cache: 12 MB I+D on chip per chip</td>
<td>Peak Pointers: 32/64-bit</td>
</tr>
<tr>
<td>Other Cache: None</td>
<td>Other Software: None</td>
</tr>
<tr>
<td>Memory: 512 GB (64 x 8 GB 2Rx4 DDR3-12800R-11, ECC, running at 1333 MHz and CL11)</td>
<td></td>
</tr>
<tr>
<td>Disk Subsystem: 1 x 300 GB SAS SAVvio 15K RPM</td>
<td></td>
</tr>
<tr>
<td>Other Hardware: None</td>
<td></td>
</tr>
</tbody>
</table>

Non-Compliant
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Results Table:

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</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
SPEC CFP2006 Result

Cisco Systems

Cisco UCS C460 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

SPECfp_rate2006 = NC
SPECfp_rate_base2006 = NC

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2014
Hardware Availability: Apr-2014
Software Availability: Sep-2013

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Platform Notes

CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State C1 Enhanced set to Disabled
Package C State Limit set to C0/C1 State
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x
System Notes program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on msc-sbrhel Fri May 2 09:21:40 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) CPU E7-4809 v2 @ 1.90GHz
4 "physical id"s (chips)
48 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 6
siblings : 12
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
physical 2: cores 0 1 2 3 4 5
physical 3: cores 0 1 2 3 4 5
cache size : 12288 KB

From /proc/meminfo

MemTotal: 529143500 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
Test date: May-2014
Hardware Availability: Apr-2014
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SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Platform Notes (Continued)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
uname -a:
Linux msc-sbrhel 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013
x86_64 x86_64 x86_64 GNU/Linux
run-level 3 May 1 14:51
SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 275G 13G 249G 5% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. C460M4.1.5.5.13.012720142211 01/27/2014
Memory:
64x 8 GB
64x 0xCE00 M393B1K70QB0-YK0 8 GB 1333 MHz 2 rank
32x NO DIMM NO DIMM
(End of data from sysinfo program)

General Notes
Environment variables set by runspec before the start of the run:

<table>
<thead>
<tr>
<th>Environment</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD_LIBRARY_PATH</td>
<td>/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh</td>
</tr>
</tbody>
</table>

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Submitted by: "Sheshgiri I (shei)" <shei@cisco.com>
Submitted: Wed May 28 03:16:44 EDT 2014

Continued on next page
SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Base Compiler Invocation

C benchmarks:

icc -m64

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
442.np: -DSPEC_CPU_LP64
443.npelm: -DSPEC_CPU_LP64
453.gromacs: -DSPEC_CPU_LP64 -nofor_main
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
467.dealII: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64
Cisco Systems

Cisco UCS C460 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

<table>
<thead>
<tr>
<th>SPECfp_rate2006 = NC</th>
<th>SPECfp_rate_base2006 = NC</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2006 license: 9019</td>
<td>Test date: May-2014</td>
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<tr>
<td>Test sponsor: Cisco Systems</td>
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<td>Software Availability: Sep-2013</td>
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</table>

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

**Base Optimization Flags**

C benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

C++ benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Fortran benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch

Benchmarks using both Fortran and C:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

**Peak Compiler Invocation**

C benchmarks (except as noted below):
icc -m64
482.sphinx3 icc -m64

C++ benchmarks (except as noted below):
icpc -m64
450.soplex icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Non-Compliant
SPEC CFP2006 Result
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Peak Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64 -nofor_main
447.dealII: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
433.milc: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -auto-ilp32
470.lbm: basepeak = yes
452.sphinx3: -xAVX -ipo -O3 -no-prec-div -opt-mem-layout-trans=3
-unroll2

C++ benchmarks:
444.namd: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -fno-alias -auto-ilp32
447.dealII: basepeak = yes
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Peak Optimization Flags (Continued)

450.soplex: -xAVX (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -prof-use (pass 2) -opt-mem-layout-trans=3 (pass 2) -opt-malloc-options=3

453.povray: -xAVX (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -prof-use (pass 2) -opt-mem-layout-trans=3 (pass 2)

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -xAVX (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -prof-use (pass 2) -opt-prefetch -inline-calloc -opt-malloc-options=3

Benchmarks using both Fortran and C:
435.gromacs: -xAVX (pass 2) -prof-gen (pass 1) -ipo (pass 2) -O3 (pass 2) -prof-use (pass 2) -opt-prefetch -auto-ilp32
436.cactusADM: basepeak = yes
454.calculix: basepeak = yes
481.wrf: -xAVX -ipo -O3 -no-prec-div -auto-ilp32
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

The flags files that were used to format this result can be browsed at:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.xml