Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.
## SPEC CFP2006 Result

Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

<table>
<thead>
<tr>
<th>SPECfp_rate2006 =</th>
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<tr>
<td>SPECfp_rate_base2006 =</td>
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**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test date:** May-2014  
**Hardware Availability:** Apr-2014  
**Software Availability:** Sep-2013

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### Hardware

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon E7-4820 v2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Characteristics:</td>
<td>Intel Turbo Boost Technology up to 2.50 GHz</td>
</tr>
<tr>
<td>CPU MHz:</td>
<td>2000</td>
</tr>
<tr>
<td>FPU:</td>
<td>Integrated</td>
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<tr>
<td>CPU(s) enabled:</td>
<td>32 cores, 4 chips, 8 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td>CPU(s) orderable:</td>
<td>1,2,3,4 Chips</td>
</tr>
<tr>
<td>Primary Cache:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Secondary Cache:</td>
<td>256 KB I+D on chip per core</td>
</tr>
<tr>
<td>L3 Cache:</td>
<td>16 MB I+D on chip per chip</td>
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<tr>
<td>Other Cache:</td>
<td>None</td>
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<tr>
<td>Memory:</td>
<td>512 GB (64 x 8 GB 2Rx4 PC3-12800R-11, ECC, running at 1333 MHz and CL11)</td>
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<tr>
<td>Disk Subsystem:</td>
<td>1 x 300 GB SAS SAVVA 15K RPM</td>
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<td>Other Hardware:</td>
<td>None</td>
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### Software

<table>
<thead>
<tr>
<th>Operating System:</th>
<th>Red Hat Enterprise Linux Server release 6.4 (Santiago)</th>
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</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux; Fortran: Version 14.0.0.080 of Intel Fortran Studio XE for Linux</td>
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<td>Auto Parallel:</td>
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<td>File System:</td>
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<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers:</td>
<td>32/64-bit</td>
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<td>Peak Pointers:</td>
<td>32/64-bit</td>
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<td>Other Software:</td>
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</table>
Cisco Systems  
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)  

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Results Table:

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<th>Seconds</th>
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<tr>
<td>434.zeusmp</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

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Platform Notes

CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State Cl Enhanced set to Disabled
Package C State Limit set to C0/C1 State
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on SPECCPU-RHEL64 Thu May 1 05:02:16 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo:

model name : Intel(R) Xeon(R) CPU E7-4820 v2 @ 2.00GHz
4 "physical id" (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7
physical 2: cores 0 1 2 3 4 5 6 7
physical 3: cores 0 1 2 3 4 5 6 7
cache size : 16384 KB

From /proc/meminfo:

MemTotal: 529141664 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

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Platform Notes (Continued)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)

uname -a:
    Linux SPECCPU-RHEL64 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41 EST 2013 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Apr 30 13:50

SPEC is set to: /opt/cpu2006-1.2
Filesyste Type Siz Used %ail Use% Mounted on
/dev/sda2 ext4 275G 13G 248G 5% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. C460M4.1.5.5.13.012720142211 01/27/2014
Memory:
64x 8 GB
64x 0xCE00 M393B1K70QB0-YK0 8 GB 1333 MHz 2 rank
32x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
    LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"
Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1>/proc/sys/vm/drop_caches
runcspec command invoked through numactl i.e.:
umactl --interleave=all runspec <etc>

Submitted by: "Sheshgiri I (shei)" <shei@cisco.com>
Submitted: Wed May 28 03:16:44 EDT 2014
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

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General Notes (Continued)
Submission: cpu2006-20140505-29493.sub

Base Compiler Invocation
C benchmarks:
    icc -m64
C++ benchmarks:
    icpc -m64
Fortran benchmarks:
    ifort -m64
Benchmarks using both Fortran and C:
    icc -m64 ifort -m64

Base Portability Flags
410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64 -nofor_main
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

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**Base Optimization Flags**

C benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

C++ benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Fortran benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch

Benchmarks using both Fortran and C:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

**Peak Compiler Invocation**

C benchmarks (except as noted below):
icc -m64
482.sphinx3 icc -m64

C++ benchmarks (except as noted below):
icpc -m64
450.soplex icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

Peak Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64 -nofor_main
447.dealII: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
433.milc: -xAVX -prof-gen(pass 1) -ipo(pass 2) -03(pass 2)
          -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
          -prof-use(pass 2) -auto-ilp32
470.lbm: basepeak = yes
482.sphinx: -xAVX -ipo -03 -no-prec-div -opt-mem-layout-trans=3
          -unroll2

C++ benchmarks:
444.namd: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -03(pass 2)
          -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
          -prof-use(pass 2) -fno-alias -auto-ilp32
447.dealII: basepeak = yes

Continued on next page
Cisco Systems

Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

SPEC CFP2006 Result

Cisco Systems

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Peak Optimization Flags (Continued)

450.soplex: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-:prof-use(pass 2) -opt-mem-layout-trans=3(pass 2)
-pret-malloc-options=3

453.povray: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-:prof-use(pass 2) -opt-mem-layout-trans=3(pass 2)
-pret-malloc-options=3

Fortran benchmarks:

410.bwaves: basepeak = yes

416.gamess: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-:prof-use(pass 2) -opt-mem-layout-trans=3(pass 2)
-pret-malloc-options=3

434.zeusmp: basepeak = yes

437.leslie3d: -xAVX -ipo -O3 -no-prec-div -opt-prefetch

459.GemsFDTD: basepeak = yes

465.tonto: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-:prof-use(pass 2) -opt-mem-layout-trans=3(pass 2)
-pret-malloc-options=3

Benchmarks using both Fortran and C:

435.gromacs: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-:prof-use(pass 2) -opt-mem-layout-trans=3(pass 2)
-pret-malloc-options=3

436.cactusADM: basepeak = yes

454.calculix: basepeak = yes

481.wrf: -xAVX -ipo -O3 -no-prec-div -auto-ilp32

Non-Compliant
### SPEC CFP2006 Result

**Cisco Systems**  
Cisco UCS C460 M4 (Intel Xeon E7-4820 v2, 1.90 GHz)

<table>
<thead>
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<th>SPECfp_rate2006</th>
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<tbody>
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- **CPU2006 license:** 9019  
- **Test sponsor:** Cisco Systems  
- **Tested by:** Cisco Systems

**Test date:** May-2014  
**Hardware Availability:** Apr-2014  
**Software Availability:** Sep-2013

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The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.xml](http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.  
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