Cisco Systems
Cisco UCS C24 M3 (Intel Xeon E5-2420 v2, 2.20 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
- CPU Name: Intel Xeon E5-2420 v2
- CPU Characteristics: Intel Turbo Boost Technology up to 2.70 GHz
- CPU MHz: 2200
- FPU: Integrated
- CPU(s) enabled: 12 cores, 2 chips, 6 cores/chip, 2 threads/core
- CPU(s) orderable: 1.2 chip
- Primary Cache: 32 KB I + 32 KB D on chip per core
- Secondary Cache: 256 KB I+D on chip per core
- L3 Cache: 15 MB I+D on chip per chip
- Other Cache: None
- Memory: 96 GB (12 x 8 GB 2Rx4 PC3L-12800R-11, ECC)
- Disk Subsystem: 1 X 600 GB 10000 RPM SAS
- Other Hardware: None

Software
- Operating System: Red Hat Enterprise Linux Server release 6.5 (Santiago)
- Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
- Auto Parallel: No
- File System: ext4
- System State: Run level 3 (multi-user)
- Base Pointers: 32-bit
- Peak Pointers: 32/64-bit
- Other Software: Microquill SmartHeap V10.0

SPECint®_rate2006 = 440
SPECint_rate_base2006 = 423
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SPEC CINT2006 Result

SPECint_rate2006 = 440
SPECint_rate_base2006 = 423

Results Table

<table>
<thead>
<tr>
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<td>483.xalancbmk</td>
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<td>467</td>
<td>356</td>
<td>465</td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Enabled
CPU Power State C1 Enhanced set to Disabled
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
DRAM Refresh Rate Set to 1x
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on SPEC-RHEL6.5 Wed May 28 18:40:16 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

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Platform Notes (Continued)

model name : Intel(R) Xeon(R) CPU E5-2420 v2 @ 2.20GHz  
2 "physical id"s (chips)  
24 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The  
following excerpts from /proc/cpuinfo might not be reliable. Use with  
caution.)  
cpu cores : 6  
siblings : 12  
physical 0: cores 0 1 2 3 4 5  
physical 1: cores 0 1 2 3 4 5  
cache size : 15360 KB

From /proc/meminfo  
MemTotal: 98988712 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d  
Red Hat Enterprise Linux Server release 6.5 (Santiago)

From /etc/*release* /etc/*version*  
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)  
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)  

uname -a:  
Linux SPEC-RHEL6.5 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54 EST 2013  
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 28 18:26

SPEC is set to: /opt/cpu2006-1.2  
filesystem Type Size Used Avail Use% Mounted on  
/dev/sda2  ext4 549G 19G 503G 4% /

Additional information from dmidecode:  
BIOS Cisco Systems, Inc. C22M3.1.5.7.0.042820140508 04/28/2014  
Memory:  
12x 0xCE00 M393B1K70DH0-YK0 8 GB 1600 MHz 2 rank

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:  
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB  
memory using RedHat EL 6.4  
Transparent Huge Pages enabled with:  
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled

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Test date: May-2014
Hardware Availability: Feb-2014
Software Availability: Mar-2014

General Notes (Continued)
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
umactl --interleave=all runspec <etc>

Submitted_by: "Vijay Durairaj (vijd)" <vijd@cisco.com>
Submitted: Thu May 29 17:11:15 EDT 2014
Submission: cpu2006-20140529-29692.sub

Base Compiler Invocation
C benchmarks:
\texttt{icc}  -m32

C++ benchmarks:
\texttt{icpc}  -m32

Base Portability Flags
400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags
C benchmarks:
-xSSE4.2  -ipo  -O3  -no-prec-div  -opt-prefetch  -opt-mem-layout-trans=3

C++ benchmarks:
-xSSE4.2  -ipo  -O3  -no-prec-div  -opt-prefetch  -opt-mem-layout-trans=3
-Wl,-z,muldefs -L/sh -lsmartheap

Base Other Flags
C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation
C benchmarks (except as noted below):
\texttt{icc}  -m32

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Peak Compiler Invocation (Continued)

400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xSSE4.2 -ipo -03 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -03 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-03(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll14 -auto-ilp32

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### Peak Optimization Flags (Continued)

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<th>C++ benchmarks:</th>
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<tbody>
<tr>
<td>462.libquantum: basepeak = yes</td>
</tr>
<tr>
<td>464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll2 -ansi-alias</td>
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<tr>
<td>471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs -L/sh -lsmartheap</td>
</tr>
<tr>
<td>473.astar: basepeak = yes</td>
</tr>
<tr>
<td>483.xalancbmk: basepeak = yes</td>
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### Peak Other Flags

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The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Originally published on 18 June 2014.