Cisco Systems

Cisco UCS C240 M4 (Intel Xeon E5-2623 v3 @ 3.00GHz)

SPECint\_rate2006 = 426
SPECint\_rate\_base2006 = 413

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
CPU Name: Intel Xeon E5-2623 v3
CPU Characteristics: Intel Turbo Boost Technology up to 3.50 GHz
CPU MHz: 3000
FPU: Integrated
CPU(s) enabled: 8 cores, 2 chips, 4 cores/chip, 2 threads/core
CPU(s) orderable: 1.2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 10 MB I+D on chip per chip
Other Cache: None
Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2133P-R, running at 1866 MHz)
Disk Subsystem: 1 x 300GB SAS, 15K RPM
Other Hardware: None

Hardware

Software

Operating System: Red Hat Enterprise Linux Server release 6.5 (Santiago)
Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0

Test date: Dec-2014
Hardware Availability: Sep-2014
Software Availability: Nov-2013

Software Availability: Nov-2013
Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2623 v3 @ 3.00GHz)

CPU2006 license: 9019
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>16</td>
<td>509</td>
<td>307</td>
<td>502</td>
<td>311</td>
<td>405</td>
<td>310</td>
<td>413</td>
<td>379</td>
<td>415</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>16</td>
<td>793</td>
<td>195</td>
<td>793</td>
<td>195</td>
<td>794</td>
<td>194</td>
<td>760</td>
<td>203</td>
<td>760</td>
</tr>
<tr>
<td>403.gcc</td>
<td>16</td>
<td>416</td>
<td>310</td>
<td>412</td>
<td>313</td>
<td>419</td>
<td>307</td>
<td>420</td>
<td>307</td>
<td>416</td>
</tr>
<tr>
<td>429.mcf</td>
<td>16</td>
<td>266</td>
<td>549</td>
<td>264</td>
<td>552</td>
<td>265</td>
<td>552</td>
<td>266</td>
<td>549</td>
<td>264</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>16</td>
<td>615</td>
<td>273</td>
<td>616</td>
<td>272</td>
<td>615</td>
<td>273</td>
<td>601</td>
<td>279</td>
<td>600</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>16</td>
<td>249</td>
<td>600</td>
<td>244</td>
<td>611</td>
<td>246</td>
<td>606</td>
<td>243</td>
<td>615</td>
<td>242</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>16</td>
<td>658</td>
<td>294</td>
<td>661</td>
<td>293</td>
<td>658</td>
<td>294</td>
<td>647</td>
<td>299</td>
<td>648</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>16</td>
<td>77.1</td>
<td>4300</td>
<td>77.6</td>
<td>4270</td>
<td>77.5</td>
<td>4280</td>
<td>77.1</td>
<td>4300</td>
<td>77.6</td>
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<tr>
<td>464.h264ref</td>
<td>16</td>
<td>721</td>
<td>491</td>
<td>744</td>
<td>476</td>
<td>717</td>
<td>494</td>
<td>700</td>
<td>506</td>
<td>706</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>16</td>
<td>465</td>
<td>215</td>
<td>469</td>
<td>213</td>
<td>467</td>
<td>214</td>
<td>440</td>
<td>227</td>
<td>442</td>
</tr>
<tr>
<td>473.astar</td>
<td>16</td>
<td>481</td>
<td>234</td>
<td>485</td>
<td>232</td>
<td>483</td>
<td>233</td>
<td>481</td>
<td>234</td>
<td>485</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>16</td>
<td>235</td>
<td>469</td>
<td>236</td>
<td>469</td>
<td>235</td>
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<td>469</td>
<td>235</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
CPU performance set to HPC
Power Technology set to Custom
Processor Power State C6 set to Disabled
Energy Performance BIAS setting set to Performance
Memory RAS configuration set to Maximum Performance
Snoop Mode set to Early Snoop
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 $$ e86d102572650a6e4d596a3cee98f191 running on rhe165 Wed Dec 10 08:50:46 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2623 v3 @ 3.00GHz
2 "physical id"s (chips)
Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2623 v3 @ 3.00GHz)

<table>
<thead>
<tr>
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</tr>
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CPU2006 license: 9019  Test date: Dec-2014
Test sponsor: Cisco Systems  Hardware Availability: Sep-2014
Tested by: Cisco Systems  Software Availability: Nov-2013

Platform Notes (Continued)

16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 4
  siblings : 8
  physical 0: cores 0 1 2 3
  physical 1: cores 0 1 2 3
  cache size : 10240 KB

From /proc/meminfo
  MemTotal: 264260856 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.5 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)

uname -a:
  Linux rhel65 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54 EST 2013 x86_64
  x86_64 x86_64 GNU/Linux

run-level 3 Dec 10 08:49

SPEC is set to: /opt/cpu2006-1.2
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sdb1 ext4 245G 19G 215G 8% /

Additional information from dmidecode:
  BIOS Cisco Systems, Inc. C240M4.2.0.3c.0.091920142008 09/19/2014
  Memory:
    16x 0xCE00 M393A2G40DB0-CPB 16 GB 1866 MHz 2 rank
    8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
  LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB
memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:

Continued on next page
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Test date: Dec-2014
Hardware Availability: Sep-2014
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General Notes (Continued)

```
echo 1>/proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:
icc -m32

C++ benchmarks:
icpc -m32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ip0 -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ip0 -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32

400.perlbench: icc -m64

Continued on next page
Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2623 v3 @ 3.00GHz)

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Peak Compiler Invocation (Continued)

401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll12 -auto-ilp32

458.sjeng: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto-ilp32

462.libquantum: basepeak = yes

Continued on next page
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
Test date: Dec-2014
Hardware Availability: Sep-2014
Software Availability: Nov-2013

Peak Optimization Flags (Continued)

464.h264ref: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.xml

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