Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2683 v3 @ 2.00GHz)

SPECint\textsubscript{rate}\textsubscript{2006} = 1100
SPECint\textsubscript{rate}_base\textsubscript{2006} = 1070

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2014
Hardware Availability: Sep-2014
Software Availability: Nov-2013

**Hardware**
- CPU Name: Intel Xeon E5-2683 v3
- CPU Characteristics: Intel Turbo Boost Technology up to 3.00 GHz
- CPU MHz: 2000
- FPU: Integrated
- CPU(s) enabled: 28 cores, 2 chips, 14 cores/chip, 2 threads/core
- CPU(s) orderable: 1.2 chips
- Primary Cache: 32 KB I + 32 KB D on chip per core
- Secondary Cache: 256 KB I+D on chip per core
- L3 Cache: 35 MB I+D on chip per chip
- Other Cache: None
- Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2133P-R)
- Disk Subsystem: 1 x 600GB SAS, 10K RPM
- Other Hardware: None

**Software**
- Operating System: Red Hat Enterprise Linux Server release 6.5 (Santiago)
- Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
- Auto Parallel: No
- File System: ext4
- System State: Run level 3 (multi-user)
- Base Pointers: 32-bit
- Peak Pointers: 32/64-bit
- Other Software: Microquill SmartHeap V10.0
### Cisco Systems

Cisco UCS B200 M4 (Intel Xeon E5-2683 v3 @ 2.00GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>56</td>
<td>656</td>
<td>834</td>
<td>659</td>
<td>831</td>
<td>658</td>
<td>831</td>
<td>56</td>
<td>536</td>
<td>1020</td>
<td>536</td>
<td>1020</td>
<td>538</td>
<td>1020</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>56</td>
<td>1001</td>
<td>540</td>
<td>1003</td>
<td>539</td>
<td>1003</td>
<td>539</td>
<td>56</td>
<td>960</td>
<td>563</td>
<td>959</td>
<td>563</td>
<td>959</td>
<td>563</td>
</tr>
<tr>
<td>403.gcc</td>
<td>56</td>
<td>548</td>
<td>823</td>
<td>547</td>
<td>823</td>
<td>554</td>
<td>814</td>
<td>56</td>
<td>554</td>
<td>814</td>
<td>555</td>
<td>813</td>
<td>555</td>
<td>813</td>
</tr>
<tr>
<td>429.mcf</td>
<td>56</td>
<td>347</td>
<td>1470</td>
<td>345</td>
<td>1480</td>
<td>346</td>
<td>1480</td>
<td>56</td>
<td>347</td>
<td>1470</td>
<td>345</td>
<td>1480</td>
<td>346</td>
<td>1480</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>56</td>
<td>812</td>
<td>724</td>
<td>811</td>
<td>724</td>
<td>811</td>
<td>724</td>
<td>56</td>
<td>791</td>
<td>743</td>
<td>792</td>
<td>742</td>
<td>792</td>
<td>742</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>56</td>
<td>355</td>
<td>1480</td>
<td>355</td>
<td>1470</td>
<td>357</td>
<td>1460</td>
<td>56</td>
<td>352</td>
<td>1480</td>
<td>351</td>
<td>1490</td>
<td>355</td>
<td>1470</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>56</td>
<td>879</td>
<td>771</td>
<td>879</td>
<td>771</td>
<td>879</td>
<td>771</td>
<td>56</td>
<td>851</td>
<td>796</td>
<td>852</td>
<td>795</td>
<td>852</td>
<td>796</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>56</td>
<td>117</td>
<td>9000</td>
<td>117</td>
<td>9940</td>
<td>117</td>
<td>9950</td>
<td>56</td>
<td>117</td>
<td>9000</td>
<td>117</td>
<td>9940</td>
<td>117</td>
<td>9950</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>56</td>
<td>985</td>
<td>1260</td>
<td>999</td>
<td>1240</td>
<td>981</td>
<td>1260</td>
<td>56</td>
<td>967</td>
<td>1280</td>
<td>961</td>
<td>1290</td>
<td>956</td>
<td>1300</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>56</td>
<td>585</td>
<td>598</td>
<td>587</td>
<td>596</td>
<td>586</td>
<td>598</td>
<td>56</td>
<td>567</td>
<td>618</td>
<td>564</td>
<td>620</td>
<td>564</td>
<td>620</td>
</tr>
<tr>
<td>473.astar</td>
<td>56</td>
<td>686</td>
<td>573</td>
<td>688</td>
<td>571</td>
<td>691</td>
<td>569</td>
<td>56</td>
<td>686</td>
<td>573</td>
<td>688</td>
<td>571</td>
<td>691</td>
<td>569</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>56</td>
<td>343</td>
<td>1130</td>
<td>344</td>
<td>1120</td>
<td>344</td>
<td>1120</td>
<td>56</td>
<td>343</td>
<td>1130</td>
<td>344</td>
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### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

CPU performance set to HPC  
Power Technology set to Custom  
Processor Power State C6 set to Disabled  
Energy Performance set to Performance  
Memory RAS configuration set to Maximum Performance

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818  
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191  
running on rhe165new Mon Dec 8 12:06:53 2014

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:  
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) CPU E5-2683 v3 @ 2.00GHz  
2 "physical id"s (chips)  
56 "processors"

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Platform Notes (Continued)

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 14
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14

cache size : 17920 KB

From /proc/meminfo
MemTotal: 264255552 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/unr/sbin/lsb_release -d
Red Hat Enterprise Linux Server release 6.5 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)

uname -a:
Linux rhel65new 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54 EST 2013
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 8 12:03

SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 550G 14G 508G 3% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. B200M4.2.2.2.30.071820140250 07/18/2014
Memory:
16x 0xCE00 M393A2G40DB0-CPB 16 GB 2133 MHz 2 rank
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
Cisco Systems
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Software Availability: Nov-2013

General Notes (Continued)
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation
C benchmarks:
  icc  -m32
C++ benchmarks:
  icpc -m32

Base Portability Flags
  400.perlbench: -DSPEC_CPU_LINUX_IA32
  462.libquantum: -DSPEC_CPU_LINUX
  483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags
C benchmarks:
  -xCORE-AVX2  -ipo  -O3  -no-prec-div  -opt-prefetch
  -opt-mem-layout-trans=3
C++ benchmarks:
  -xCORE-AVX2  -ipo  -O3  -no-prec-div  -opt-prefetch
  -opt-mem-layout-trans=3  -Wl,-z,muldefs  -L/sh -lsmartheap

Base Other Flags
C benchmarks:
  403.gcc: -Dalloca=_alloca

Peak Compiler Invocation
C benchmarks (except as noted below):
  icc  -m32
  400.perlbench: icc -m64
  401.bzip2: icc -m64

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Cisco UCS B200 M4 (Intel Xeon E5-2683 v3 @ 2.00GHz)

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Hardware Availability: Sep-2014
Software Availability: Nov-2013

Peak Compiler Invocation (Continued)

456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
400.perlbench: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32
401.bzip2: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias
403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div
429.mcf: basepeak = yes
445.gobmk: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3
456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
458.sjeng: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4 -auto-ilp32
462.libquantum: basepeak = yes
464.h264ref: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

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Peak Optimization Flags (Continued)

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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