## Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650 v3 @ 3.00GHz)

<table>
<thead>
<tr>
<th>SPECint_rate2006</th>
<th>=</th>
<th>848</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>=</td>
<td>821</td>
</tr>
</tbody>
</table>

**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Hardware Availability:** Sep-2014  
**Software Availability:** Nov-2013

### Hardware

<table>
<thead>
<tr>
<th>Property</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon E5-2650 v3</td>
</tr>
<tr>
<td>CPU Characteristics</td>
<td>Intel Turbo Boost Technology up to 3.00 GHz</td>
</tr>
<tr>
<td>CPU MHz</td>
<td>2300</td>
</tr>
<tr>
<td>FPU</td>
<td>Integrated</td>
</tr>
<tr>
<td>CPU(s) enabled</td>
<td>20 cores, 2 chips, 10 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td>CPU(s) orderable</td>
<td>1.2 chips</td>
</tr>
<tr>
<td>Primary Cache</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Secondary Cache</td>
<td>256 KB I+D on chip per core</td>
</tr>
<tr>
<td>L3 Cache</td>
<td>25 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other Cache</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>256 GB (16 x 16 GB 2Rx4 PC4-2133P-R)</td>
</tr>
<tr>
<td>Disk Subsystem</td>
<td>1 x 300GB SAS, 15K RPM</td>
</tr>
<tr>
<td>Other Hardware</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Property</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System</td>
<td>Red Hat Enterprise Linux Server release 6.5 (Santiago)</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux</td>
</tr>
<tr>
<td>Auto Parallel</td>
<td>No</td>
</tr>
<tr>
<td>File System</td>
<td>ext4</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>32-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other Software</td>
<td>Microquill SmartHeap V10.0</td>
</tr>
</tbody>
</table>

---

Copyright 2006-2015 Standard Performance Evaluation Corporation

info@spec.org  
http://www.spec.org/
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650 v3 @ 3.00GHz)

SPECint_rate2006 = 848
SPECint_rate_base2006 = 821

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Feb-2015
Hardware Availability: Sep-2014
Software Availability: Nov-2013

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>40</td>
<td>632</td>
<td>618</td>
<td>638</td>
<td>613</td>
<td>636</td>
<td>615</td>
<td>40</td>
<td>519</td>
<td>752</td>
<td>519</td>
<td>753</td>
<td>519</td>
<td>753</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>40</td>
<td>964</td>
<td>400</td>
<td>965</td>
<td>400</td>
<td>966</td>
<td>400</td>
<td>40</td>
<td>921</td>
<td>419</td>
<td>923</td>
<td>418</td>
<td>923</td>
<td>418</td>
</tr>
<tr>
<td>403.gcc</td>
<td>40</td>
<td>515</td>
<td>625</td>
<td>517</td>
<td>623</td>
<td>521</td>
<td>618</td>
<td>40</td>
<td>522</td>
<td>617</td>
<td>516</td>
<td>623</td>
<td>520</td>
<td>619</td>
</tr>
<tr>
<td>429.mcf</td>
<td>40</td>
<td>323</td>
<td>1130</td>
<td>322</td>
<td>1130</td>
<td>323</td>
<td>1130</td>
<td>40</td>
<td>323</td>
<td>1130</td>
<td>322</td>
<td>1130</td>
<td>323</td>
<td>1130</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>40</td>
<td>779</td>
<td>539</td>
<td>779</td>
<td>539</td>
<td>779</td>
<td>539</td>
<td>40</td>
<td>761</td>
<td>552</td>
<td>760</td>
<td>552</td>
<td>760</td>
<td>552</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>40</td>
<td>316</td>
<td>1180</td>
<td>318</td>
<td>1170</td>
<td>319</td>
<td>1170</td>
<td>40</td>
<td>313</td>
<td>1190</td>
<td>315</td>
<td>1190</td>
<td>314</td>
<td>1190</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>40</td>
<td>846</td>
<td>572</td>
<td>846</td>
<td>572</td>
<td>846</td>
<td>572</td>
<td>40</td>
<td>818</td>
<td>591</td>
<td>819</td>
<td>591</td>
<td>818</td>
<td>591</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>40</td>
<td>99.7</td>
<td>8320</td>
<td>99.7</td>
<td>8320</td>
<td>100</td>
<td>8280</td>
<td>40</td>
<td>99.7</td>
<td>8320</td>
<td>99.7</td>
<td>8320</td>
<td>100</td>
<td>8280</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>40</td>
<td>941</td>
<td>940</td>
<td>929</td>
<td>953</td>
<td>918</td>
<td>964</td>
<td>40</td>
<td>905</td>
<td>978</td>
<td>910</td>
<td>972</td>
<td>927</td>
<td>955</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>40</td>
<td>537</td>
<td>466</td>
<td>540</td>
<td>463</td>
<td>541</td>
<td>463</td>
<td>40</td>
<td>509</td>
<td>491</td>
<td>510</td>
<td>490</td>
<td>510</td>
<td>490</td>
</tr>
<tr>
<td>473.astar</td>
<td>40</td>
<td>626</td>
<td>449</td>
<td>627</td>
<td>447</td>
<td>627</td>
<td>448</td>
<td>40</td>
<td>626</td>
<td>449</td>
<td>627</td>
<td>447</td>
<td>627</td>
<td>448</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>40</td>
<td>302</td>
<td>913</td>
<td>302</td>
<td>913</td>
<td>302</td>
<td>914</td>
<td>40</td>
<td>302</td>
<td>913</td>
<td>302</td>
<td>913</td>
<td>302</td>
<td>914</td>
</tr>
</tbody>
</table>

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
CPU Performance set to HPC
Power Technology set to Custom
Processor Power State C6 set to Disabled
Energy Performance BIAS setting set to Performance
Memory RAS configuration set to Maximum Performance
QPI Snoop Mode set to Early Snoop
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
running on localhost.localdomain Wed Feb 11 16:18:38 2015

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2650 v3 @ 2.30GHz
2 "physical id"s (chips)
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650 v3 @ 3.00GHz)

SPECint_rate2006 = 848
SPECint_rate_base2006 = 821

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
cache size : 25600 KB

From /proc/meminfo
MemTotal: 264258524 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.5 (Santiago)

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.5 (Santiago)

uname -a:
Linux localhost.localdomain 2.6.32-431.el6.x86_64 #1 SMP Sun Nov 10 22:19:54
EST 2013 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Feb 11 16:15

SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 ext4 193G 12G 172G 7% /

Additional information from dmidecode:
BIOS Cisco Systems, Inc. B200M4.2.2.3d.0.111420141438 11/14/2014
Memory:
16x 0xCE00 M393A2G40DB0-CPB 16 GB 2133 MHz 2 rank
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i7-860 CPU + 8GB memory using RedHat EL 6.4
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
Filesystem page cache cleared with:

Continued on next page
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650 v3 @ 3.00GHz)

SPECint_rate2006 = 848
SPECint_rate_base2006 = 821

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Feb-2015
Tested by: Cisco Systems
Hardware Availability: Sep-2014
Software Availability: Nov-2013

General Notes (Continued)

    echo 1>/proc/sys/vm/drop_caches
    runspec command invoked through numactl i.e.:
    numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
    icc -m32
C++ benchmarks:
    icpc -m32

Base Portability Flags

    400.perlbench: -DSPEC_CPU_LINUX_IA32
    462.libquantum: -DSPEC_CPU_LINUX
    483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
    -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
    -opt-mem-layout-trans=3
C++ benchmarks:
    -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
    -opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap

Base Other Flags

C benchmarks:
    403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
    icc -m32
    400.perlbench: icc -m64

Continued on next page
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650 v3 @ 3.00GHz)

SPECint_rate2006 = 848
SPECint_rate_base2006 = 821

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Feb-2015
Hardware Availability: Sep-2014
Software Availability: Nov-2013

Peak Compiler Invocation (Continued)

401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-auto-ilp32

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div

429.mcf: basepeak = yes

445.gobmk: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4 -auto-ilp32

462.libquantum: basepeak = yes

Continued on next page
Cisco Systems
Cisco UCS B200 M4 (Intel Xeon E5-2650 v3 @ 3.00GHz)  

SPECint_rate2006 = 848  
SPECint_rate_base2006 = 821

CPU2006 license: 9019  
Test sponsor: Cisco Systems  
Tested by: Cisco Systems  

Test date: Feb-2015  
Hardware Availability: Sep-2014  
Software Availability: Nov-2013

Peak Optimization Flags (Continued)

464.h264ref: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
-o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)  
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
-o3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)  
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs  
-L/sh -lsmartheap

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html  
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml  
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.xml

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.  
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.  
Originally published on 10 March 2015.