Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-8890 v3 @ 2.50 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPECint_rate2006 = 2870
SPECint_rate_base2006 = 2770

Test date: May-2015
Hardware Availability: Apr-2014
Software Availability: Sep-2014

Software
Operating System: SUSE Linux Enterprise Server 12 (x86_64) 3.12.28-4-default
Compiler: C/C++: Version 15.0.0.090 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0

Hardware
CPU Name: Intel Xeon E7-8890 v3
CPU Characteristics: Intel Turbo Boost Technology up to 3.30 GHz
CPU MHz: 2500
FPU: Integrated
CPU(s) enabled: 72 cores, 4 chips, 18 cores/chip, 2 threads/core
CPU(s) orderable: 1,2,3,4 Chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 45 MB I+D on chip per chip
Other Cache: None
Memory: 1 TB (64 x 16 GB 2Rx4 PC4-2133P-R, running at 1600 MHz)
Disk Subsystem: 1 x 400 GB 6Gb/s SSD
Other Hardware: None
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Results Table

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<td>344</td>
<td>2890</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
Power Technology set to Performance
CPU Power State C6 set to Disabled
CPU Power State C1 set to Disabled
Package C State Limit set to C0/C1 State
Energy Performance policy set to Balanced Performance
Memory Power saving mode set to Disabled
LV DDR Mode set to Performance mode
Memory RAS configuration set to Maximum Performance
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
running on linux-cfac Tue May 12 16:39:31 2015

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

Continued on next page
**Cisco Systems**
Cisco UCS C460 M4 (Intel Xeon E7-8890 v3 @ 2.50 GHz)

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**Platform Notes (Continued)**

- **model name**: Intel(R) Xeon(R) CPU E7-8890 v3 @ 2.50GHz  
  4 "physical id"s (chips)  
  144 "processors"
- **cores, siblings**: (Caution: counting these is hw and system dependent. The following excerpts from \texttt{/proc/cpuinfo} might not be reliable. Use with caution.)
  - cpu cores : 18
  - siblings : 36
  - physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  - physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  - physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  - physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
- **cache size**: 46080 KB

From \texttt{/proc/meminfo}
- MemTotal: 1058822424 kB
- HugePages\_Total: 0
- Hugepagesize: 2048 kB

From \texttt{/etc/*release* /etc/*version*}
- SuSE\_release:
  - SUSE Linux Enterprise Server 12 (x86\_64)
  - VERSION = 12
  - PATCHLEVEL = 0
  - # This file is deprecated and will be removed in a future service pack or release.
  - # Please check \texttt{/etc/os-release} for details about this release.
- os\_release:
  - NAME="SLES"
  - VERSION="12"
  - VERSION\_ID="12"
  - PRETTY\_NAME="SUSE Linux Enterprise Server 12"
  - ID="sles"
  - ANSI\_COLOR="0;32"
  - CPE\_NAME="cpe:/o:suse:sles:12"

uname -a:
- Linux linux-cfac 3.12.28-4-default #1 SMP Thu Sep 25 17:02:34 UTC 2014 (9879bd4) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 May 12 15:01

SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use\% Mounted on
/dev/sdb1 xfs 181G 34G 147G 19% /

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Continued on next page
Cisco Systems
Cisco UCS C460 M4 (Intel Xeon E7-8890 v3 @ 2.50 GHz)

SPECint_rate2006 = 2870
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)
BIOS Cisco Systems, Inc. C460M4.2.0.4.20.040420150215 04/04/2015
Memory:
  64x 0xCE00 M393A2G40DB0-CPB 16 GB 2 rank 1600 MHz
  32x NO DIMM NO DIMM 1600 MHz
(End of data from sysinfo program)

General Notes
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i5-4670K CPU + 16GB memory using RedHat EL 7.0
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
umactl --interleave=all runspec <etc>

Base Compiler Invocation
C benchmarks:
icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
C++ benchmarks:
icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32

Base Portability Flags
400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags
C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3
C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap
**SPEC CINT2006 Result**

**Cisco Systems**
Cisco UCS C460 M4 (Intel Xeon E7-8890 v3 @ 2.50 GHz)

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| SPECint_rate_base2006 = 2770 |

**Base Other Flags**

C benchmarks:

403.gcc: `-Dalloca=_alloca`

**Peak Compiler Invocation**

C benchmarks (except as noted below):

```bash
icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
```

400.perlbench: `icc -m64`

401.bzip2: `icc -m64`

456.hmmer: `icc -m64`

458.sjeng: `icc -m64`

C++ benchmarks:

```bash
icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
```

**Peak Portability Flags**

400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`

401.bzip2: `-DSPEC_CPU_LP64`

456.hmmer: `-DSPEC_CPU_LP64`

458.sjeng: `-DSPEC_CPU_LP64`

462.libquantum: `-DSPEC_CPU_LINUX`

483.xalancbmk: `-DSPEC_CPU_LINUX`

**Peak Optimization Flags**

C benchmarks:

400.perlbench: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32`

401.bzip2: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias`

403.gcc: `-xCORE-AVX2 -ipo -O3 -no-prec-div`

Continued on next page
Cisco Systems
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SPEC CINT2006 Result

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Peak Optimization Flags (Continued)

429.mcf: basepeak = yes

445.gobmk: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
-L/sh -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.20150505.xml
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For other inquiries, please contact webmaster@spec.org.

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