Cisco Systems
Cisco UCS C3160 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Software
Operating System: SUSE Linux Enterprise Server 12 (x86_64)
3.12.28-4-default
Compiler: C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux
Auto Parallel: No
File System: ext4
System State: Run level 3 (multi-user)
Base Pointers: 32-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.0

Hardware
CPU Name: Intel Xeon E5-2620 v2
CPU Characteristics: Intel Turbo Boost Technology up to 2.60 GHz
CPU MHz: 2100
FPU: Integrated
CPU(s) enabled: 12 cores, 2 chips, 6 cores/chip, 2 threads/core
CPU(s) orderable: 1.2 chip
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 15 MB I+D on chip per chip
Other Cache: None
Memory: 256 GB (16 x 16 GB 2Rx4 PC3-14900R-13, ECC, running at 1600 MHz and CL7)
Disk Subsystem: 1 X 400 GB SSD SAS
Other Hardware: None
Cisco Systems
Cisco UCS C3160 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

SPECrate2006 = 436
SPECint_rate_base2006 = 416

CPU2006 license: 9019
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Results Table

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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HT Technology = Enabled
CPU performance set to Enterprise
Power Technology set to Custom
CPU Power State C6 set to Disabled
CPU Power State C1 Enhanced set to Disabled
Energy Performance policy set to Performance
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
LV DDR Mode set to Performance-mode
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
running on linux-vedd Mon May 4 22:52:40 2015

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo
Continued on next page
Cisco Systems
Cisco UCS C3160 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

|CPU2006 license| 9019| Test date: | May-2015|
|Test sponsor:  | Cisco Systems| Hardware Availability: | Sep-2014|
|Tested by:     | Cisco Systems| Software Availability: | Sep-2014|

**SPEC CINT2006 Result**

| SPECint_rate2006 | 436|
| SPECint_rate_base2006 | 416|

Platform Notes (Continued)

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) CPU E5-2620 v2 @ 2.10GHz
- 2 "physical id"s (chips)
- 24 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  - cpu cores : 6
  - siblings : 12
  - physical 0: cores 0 1 2 3 4 5
  - physical 1: cores 0 1 2 3 4 5
- cache size : 15360 KB

From /proc/meminfo
- MemTotal: 264646116 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
- SuSE-release:
  - SUSE Linux Enterprise Server 12 (x86_64)
  - VERSION = 12
  - PATCHLEVEL = 0
  - # This file is deprecated and will be removed in a future service pack or release.
  - # Please check /etc/os-release for details about this release.

- os-release:
  - NAME="SLES"
  - VERSION="12"
  - VERSION_ID="12"
  - PRETTY_NAME="SUSE Linux Enterprise Server 12"
  - ID="sles"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:12"

- uname -a:
  - Linux linux-vedd 3.12.28-4-default #1 SMP Thu Sep 25 17:02:34 UTC 2014
  - (9879bd4) x86_64 x86_64 x86_64 GNU/Linux

- run-level 3 May 4 08:25

- SPEC is set to: /opt/cpu2006-1.2

- Filesystem Type Size Used Avail Used% Mounted on
  - /dev/sdy1 ext4 394G 11G 382G 3% /

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Cisco Systems
Cisco UCS C3160 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

SPECint_rate2006 = 436
SPECint_rate_base2006 = 416

Platform Notes (Continued)

BIOS Cisco Systems, Inc. C3160M3.2.0.2a.0.090920140606 09/09/2014
Memory:
   16x 0xAD00 HMT42GR7AFR4C-RD 16 GB 2 rank 1866 MHz, configured at 1600 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i5-4670K CPU + 16GB memory using RedHat EL 7.0
Transparent Huge Pages enabled with:
   echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
   echo 1>       /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
   numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
   icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32

C++ benchmarks:
   icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
   -xSSE4.2 -ipo -03 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3

C++ benchmarks:
   -xSSE4.2 -ipo -03 -no-prec-div -opt-prefetch -opt-mem-layout-trans=3
   -Wl,-z,muldefs -L/sh -lsmartheap
Cisco Systems
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SPECint_rate_base2006 = 416

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: May-2015
Hardware Availability: Sep-2014
Software Availability: Sep-2014

Base Other Flags
C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation
C benchmarks (except as noted below):
  icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32

Peak Portability Flags
400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Peak Optimization Flags
C benchmarks:
400.perlbench: -xsSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -auto-ilp32
401.bzip2: -xsSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -opt-prefetch -auto-ilp32 -ansi-alias
403.gcc: -xsSE4.2 -ipo -O3 -no-prec-div

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Cisco UCS C3160 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

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</tbody>
</table>

**Peak Optimization Flags (Continued)**

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
  -ansi-alias -opt-mem-layout-trans=3

456.hmmer: -xSSE4.2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll4 -auto-ilp32

462.libquantum: basepeak = yes

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
  -L/sh -lsmartheap

473.astar: basepeak = yes

483.xalancbmk: basepeak = yes

**Peak Other Flags**

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
[http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html](http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:
[http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml](http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml)
Cisco Systems
Cisco UCS C3160 M3 (Intel Xeon E5-2620 v2, 2.10 GHz)

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SPECint_rate_base2006 = 416

- **CPU2006 license:** 9019
- **Test sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Test date:** May-2015
- **Hardware Availability:** Sep-2014
- **Software Availability:** Sep-2014

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For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.

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