Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4655 v3, 2.90 GHz)

| SPECint®2006 | 61.6 |
| SPECint_base2006 | 59.8 |

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware

| CPU Name: | Intel Xeon E5-4655 v3 |
| CPU Characteristics: | Intel Turbo Boost Technology up to 3.20 GHz |
| CPU MHz: | 2900 |
| FPU: | Integrated |
| CPU(s) enabled: | 24 cores, 4 chips, 6 cores/chip |
| CPU(s) orderable: | 2,4 chip |
| Primary Cache: | 32 KB I + 32 KB D on chip per core |
| Secondary Cache: | 256 KB I+D on chip per core |
| L3 Cache: | 30 MB I+D on chip per chip |
| Other Cache: | None |
| Memory: | 512 GB (32 x 16 GB 2Rx4 PC4-2133P-R) |
| Disk Subsystem: | 1 x 300 GB SAS, 15K RPM |

Software

| Operating System: | SUSE Linux Enterprise Server 12 (x86_64) 3.12.28-4-default |
| Compiler: | C/C++: Version 15.0.0.090 of Intel C++ Studio XE for Linux |
| Auto Parallel: | Yes |
| File System: | xfs |
| System State: | Run level 3 (multi-user) |
| Base Pointers: | 32/64-bit |
| Peak Pointers: | 32/64-bit |
| Other Software: | Microquill SmartHeap V10.0 |

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info@spec.org
http://www.spec.org/
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Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>400.perlbench</td>
<td>262</td>
<td>37.3</td>
<td>262</td>
<td>37.3</td>
<td>263</td>
<td>37.1</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>418</td>
<td>23.1</td>
<td>416</td>
<td>23.2</td>
<td>418</td>
<td>23.1</td>
</tr>
<tr>
<td>403.gcc</td>
<td>236</td>
<td>34.1</td>
<td>237</td>
<td>33.9</td>
<td>237</td>
<td>34.0</td>
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<tr>
<td>429.mcf</td>
<td>144</td>
<td>63.4</td>
<td>149</td>
<td>61.2</td>
<td>145</td>
<td>62.7</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>390</td>
<td>26.9</td>
<td>391</td>
<td>26.8</td>
<td>390</td>
<td>26.9</td>
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<tr>
<td>456.hmmer</td>
<td>147</td>
<td>63.5</td>
<td>148</td>
<td>63.1</td>
<td>147</td>
<td>63.6</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>380</td>
<td>31.9</td>
<td>379</td>
<td>31.9</td>
<td>380</td>
<td>31.9</td>
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<tr>
<td>462.libquantum</td>
<td>3.45</td>
<td>6010</td>
<td>3.46</td>
<td>5990</td>
<td>3.45</td>
<td>6010</td>
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<tr>
<td>464.h264ref</td>
<td>454</td>
<td>48.7</td>
<td>454</td>
<td>48.7</td>
<td>450</td>
<td>49.2</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>170</td>
<td>36.8</td>
<td>164</td>
<td>38.1</td>
<td>169</td>
<td>37.0</td>
</tr>
<tr>
<td>473.astar</td>
<td>221</td>
<td>31.7</td>
<td>224</td>
<td>31.3</td>
<td>224</td>
<td>31.4</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>115</td>
<td>59.9</td>
<td>113</td>
<td>61.0</td>
<td>111</td>
<td>62.4</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The config file option 'submit' was used.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Configuratton:
Hyper-Threading Technology set to Disabled
CPU performance set to Enterprise
Power Technology set to Energy-Efficient
Energy Performance BIAS setting set to Balanced Performance
Memory RAS configuration set to Maximum Performance
LV DDR Mode set to Performance-mode
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
running on linux-616o Thu Jul 23 05:40:07 2015

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-4655 v3 @ 2.90GHz
4 "physical id"s (chips)
24 "processors"

Continued on next page
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Platform Notes (Continued)
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 6
  siblings : 6
  physical 0: cores 1 3 5 9 11 12
  physical 1: cores 1 3 5 9 11 12
  physical 2: cores 1 3 5 9 11 12
  physical 3: cores 1 3 5 9 11 12
  cache size : 30720 KB

From /proc/meminfo
  MemTotal: 529337924 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
    NAME="SLES"
    VERSION="12"
    VERSION_ID="12"
    PRETTY_NAME="SUSE Linux Enterprise Server 12"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12"

uname -a:
  Linux linux-616o 3.12.28-4-default #1 SMP Thu Sep 25 17:02:34 UTC 2014
  (9879bd4) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jul 22 23:56

SPEC is set to: /opt/cpu2006-1.2

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B420M4.2.2.5.0.043020152304 04/30/2015
Memory:
  32x 0xCE00 M393A2G40DB0-CPB 16 GB 2 rank 2133 MHz

Continued on next page
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Hardware Availability: Jun-2015
Software Availability: Nov-2014

Platform Notes (Continued)

16x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact,1,0"
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"
OMP_NUM_THREADS = "24"

Binaries compiled on a system with 1x Core i5-4670K CPU + 16GB memory using RedHat EL 7.0
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
  icc -m64

C++ benchmarks:
  icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
  401.bzip2: -DSPEC_CPU_LP64
  403.gcc: -DSPEC_CPU_LP64
  429.mcf: -DSPEC_CPU_LP64
  445.gobmk: -DSPEC_CPU_LP64
  456.hmmer: -DSPEC_CPU_LP64
  458.sjeng: -DSPEC_CPU_LP64
  462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
  464.h264ref: -DSPEC_CPU_LP64
  471.omnetpp: -DSPEC_CPU_LP64
  473.astar: -DSPEC_CPU_LP64
  483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
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Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-Wl,-z,muldefs -L/sh -lsmartheap64

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64

400.perlbench: icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
445.gobmk: icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32

C++ benchmarks (except as noted below):
icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32
473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LINUX
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**CPU2006 license:** 9019  
**Test date:** Jul-2015  
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**Hardware Availability:** Jun-2015  
**Tested by:** Cisco Systems  
**Software Availability:** Nov-2014  

### Peak Optimization Flags

**C benchmarks:**

400.perlbench: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-prefetch -ansi-alias`

401.bzip2: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div -prof-use(pass 2) -auto-ilp32
-opt-prefetch -ansi-alias`

403.gcc: `-xCORE-AVX2 -ipo -O3 -no-prec-div -inline-calloc
-opt-malloc-options=3 -auto-ilp32`

429.mcf: `-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
-opt-prefetch -auto-p32`

445.gobmk: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
-ansi-alias`

456.hmmer: `-xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
-ansi-alias`

458.sjeng: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-unroll4`

462.libquantum: `basepeak = yes`

464.h264ref: `basepeak = yes`

### Peak Other Flags

**C++ benchmarks:**

471.omnetpp: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
-O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
-opt-ra-region-strategy=block -ansi-alias
-Wl,-z,muldefs -L/sh -lsmartheap`

473.astar: `-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-auto-p32 -Wl,-z,muldefs -L/sh -lsmartheap64`

483.xalancbmk: `-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-ansi-alias -Wl,-z,muldefs -L/sh -lsmartheap`
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Peak Other Flags (Continued)

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.20150812.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revC.20150812.xml

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