## Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

<table>
<thead>
<tr>
<th>CPU2006 license:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test date:</td>
<td>Aug-2015</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Jun-2015</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Nov-2014</td>
</tr>
</tbody>
</table>

### SPECint Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECint_rate2006</th>
<th>SPECint_rate_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>16100</td>
<td>1850</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>903</td>
<td>1770</td>
</tr>
<tr>
<td>403.gcc</td>
<td>1370</td>
<td></td>
</tr>
<tr>
<td>429.mcf</td>
<td>2390</td>
<td></td>
</tr>
<tr>
<td>445.gobmk</td>
<td>1200</td>
<td></td>
</tr>
<tr>
<td>456.hmmer</td>
<td>2560</td>
<td></td>
</tr>
<tr>
<td>458.sjeng</td>
<td>1320</td>
<td></td>
</tr>
<tr>
<td>462.libquantum</td>
<td>1270</td>
<td></td>
</tr>
<tr>
<td>464.h264ref</td>
<td>2120</td>
<td></td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>1020</td>
<td></td>
</tr>
<tr>
<td>473.astar</td>
<td>983</td>
<td></td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>1910</td>
<td></td>
</tr>
</tbody>
</table>

**SPECint_rate_base2006 = 1770**

**SPECint_rate2006 = 1850**

### Hardware

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon E5-4650 v3</td>
</tr>
<tr>
<td>CPU Characteristics</td>
<td>Intel Turbo Boost Technology up to 2.80 GHz</td>
</tr>
<tr>
<td>CPU MHz</td>
<td>2100</td>
</tr>
<tr>
<td>FPU</td>
<td>Integrated</td>
</tr>
<tr>
<td>CPU(s) enabled</td>
<td>48 cores, 4 chips, 12 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td>CPU(s) orderable</td>
<td>2,4 chip</td>
</tr>
<tr>
<td>Primary Cache</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Secondary Cache</td>
<td>256 KB I+D on chip per core</td>
</tr>
<tr>
<td>L3 Cache</td>
<td>30 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other Cache</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>512 GB (32 x 16 GB 2Rx4 PC4-2133P-R)</td>
</tr>
<tr>
<td>Disk Subsystem</td>
<td>1 x 300 GB SAS, 15K RPM</td>
</tr>
<tr>
<td>Other Hardware</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System</td>
<td>SUSE Linux Enterprise Server 12 (x86_64)</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 15.0.0.0.90 of Intel C++ Studio XE for Linux</td>
</tr>
<tr>
<td>Auto Parallel</td>
<td>No</td>
</tr>
<tr>
<td>File System</td>
<td>xfs</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>32-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other Software</td>
<td>Microquill SmartHeap V10.0</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

SPECint_rate2006 = 1850
SPECint_rate_base2006 = 1770

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Aug-2015
Hardware Availability: Jun-2015
Software Availability: Nov-2014

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>96</td>
<td>731</td>
<td>1280</td>
<td>731</td>
<td>1280</td>
<td>96</td>
<td>583</td>
<td>1610</td>
<td>583</td>
<td>1610</td>
<td>583</td>
<td>1610</td>
<td>583</td>
<td>1610</td>
</tr>
<tr>
<td>bzip2</td>
<td>96</td>
<td>1075</td>
<td>862</td>
<td>1076</td>
<td>861</td>
<td>96</td>
<td>1028</td>
<td>901</td>
<td>1028</td>
<td>902</td>
<td>1029</td>
<td>901</td>
<td>1029</td>
<td>901</td>
</tr>
<tr>
<td>gcc</td>
<td>96</td>
<td>568</td>
<td>1360</td>
<td>568</td>
<td>1360</td>
<td>96</td>
<td>564</td>
<td>1370</td>
<td>565</td>
<td>1370</td>
<td>570</td>
<td>1350</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mcf</td>
<td>96</td>
<td>366</td>
<td>2390</td>
<td>366</td>
<td>2390</td>
<td>96</td>
<td>366</td>
<td>2390</td>
<td>366</td>
<td>2390</td>
<td>365</td>
<td>2400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>gobmk</td>
<td>96</td>
<td>842</td>
<td>1200</td>
<td>842</td>
<td>1200</td>
<td>96</td>
<td>835</td>
<td>1210</td>
<td>836</td>
<td>1200</td>
<td>836</td>
<td>1200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>hammer</td>
<td>96</td>
<td>349</td>
<td>2560</td>
<td>358</td>
<td>2500</td>
<td>347</td>
<td>2580</td>
<td>96</td>
<td>316</td>
<td>2830</td>
<td>317</td>
<td>2830</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sjeng</td>
<td>96</td>
<td>916</td>
<td>1270</td>
<td>916</td>
<td>1270</td>
<td>96</td>
<td>878</td>
<td>1320</td>
<td>879</td>
<td>1320</td>
<td>878</td>
<td>1320</td>
<td></td>
<td></td>
</tr>
<tr>
<td>libquantm</td>
<td>96</td>
<td>110</td>
<td>18000</td>
<td>111</td>
<td>18000</td>
<td>111</td>
<td>18000</td>
<td>96</td>
<td>110</td>
<td>18000</td>
<td>111</td>
<td>18000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>h264ref</td>
<td>96</td>
<td>1016</td>
<td>2090</td>
<td>1043</td>
<td>2040</td>
<td>96</td>
<td>1021</td>
<td>2080</td>
<td>986</td>
<td>2160</td>
<td>1004</td>
<td>2120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>omnetpp</td>
<td>96</td>
<td>615</td>
<td>975</td>
<td>619</td>
<td>970</td>
<td>620</td>
<td>968</td>
<td>96</td>
<td>587</td>
<td>1020</td>
<td>586</td>
<td>1020</td>
<td></td>
<td></td>
</tr>
<tr>
<td>astar</td>
<td>96</td>
<td>688</td>
<td>979</td>
<td>683</td>
<td>986</td>
<td>686</td>
<td>983</td>
<td>96</td>
<td>688</td>
<td>979</td>
<td>683</td>
<td>986</td>
<td></td>
<td></td>
</tr>
<tr>
<td>xalancbmk</td>
<td>96</td>
<td>347</td>
<td>1910</td>
<td>346</td>
<td>1910</td>
<td>96</td>
<td>347</td>
<td>1910</td>
<td>346</td>
<td>1920</td>
<td>346</td>
<td>1910</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Configuration:
CPU performance set to Enterprise
Power Technology set to Energy-Efficient
Energy Performance BIAS setting set to Balanced Performance
Memory RAS configuration set to Maximum Performance
LV DDR Mode set to Performance-mode
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1
running on linux-616o Fri Aug 7 11:10:23 2015

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-4650 v3 @ 2.10GHz
4 "physical id"s (chips)
Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

**SPECint_rate2006 = 1850**
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

**Platform Notes (Continued)**

96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
caution.)

- cpu cores : 12
- siblings : 24
- physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
- physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13
- physical 2: cores 0 1 2 3 4 5 8 9 10 11 12 13
- physical 3: cores 0 1 2 3 4 5 8 9 10 11 12 13

```
cache size : 30720 KB
```

From /proc/meminfo

```
MemTotal:       529329124 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From /etc/*release*/etc/*version*

```
SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 0
    # This file is deprecated and will be removed in a future service pack or
    release.
    # Please check /etc/os-release for details about this release.

os-release:
    NAME="SLES"
    VERSION="12"
    VERSION_ID="12"
    PRETTY_NAME="SUSE Linux Enterprise Server 12"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12"
```

```
uname -a:
    Linux linux-616o 3.12.28-4-default #1 SMP Thu Sep 25 17:02:34 UTC 2014
    (9879bd4) x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Aug 7 11:05
```

```
SPEC is set to: /opt/cpu2006-1.2
Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sdc2      xfs   250G  84G  167G  34% /

Additional information from dmidecode:
```

Warning: Use caution when you interpret this section. The 'dmidecode' program
reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B420M4.2.2.5.0.043020152304 04/30/2015
Memory:
```

Continued on next page
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Platform Notes (Continued)

32x 0xCE00 M393A2G40DB0-CPB 16 GB 2 rank 2133 MHz
16x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

Binaries compiled on a system with 1x Core i5-4670K CPU + 16GB memory using RedHat EL 7.0
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runcspe command invoked through numactl i.e.:
umactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32

C++ benchmarks:
icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32

Base Portability Flags

400.perlbench: -DSPEC_CPU_LINUX_IA32
462.libquantum: -DSPEC_CPU_LINUX
483.xalancbmk: -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
-opt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh -lsmartheap
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### Base Other Flags

C benchmarks:

- 403.gcc: `-Dalloca=_alloca`

### Peak Compiler Invocation

C benchmarks (except as noted below):

- `icc -m32 -L/opt/intel/composer_xe_2015/lib/ia32`
- 400.perlbench: `icc -m64`
- 401.bzip2: `icc -m64`
- 456.hmmer: `icc -m64`
- 458.sjeng: `icc -m64`

C++ benchmarks:

- `icpc -m32 -L/opt/intel/composer_xe_2015/lib/ia32`

### Peak Portability Flags

- 400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
- 401.bzip2: `-DSPEC_CPU_LP64`
- 456.hmmer: `-DSPEC_CPU_LP64`
- 458.sjeng: `-DSPEC_CPU_LP64`
- 462.libquantum: `-DSPEC_CPU_LINUX`
- 483.xalancbmk: `-DSPEC_CPU_LINUX`

### Peak Optimization Flags

C benchmarks:

- 400.perlbench: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -auto-ilp32`
- 401.bzip2: `-xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias`
- 403.gcc: `-xCORE-AVX2 -ipo -O3 -no-prec-div`

Continued on next page

Standard Performance Evaluation Corporation
info@spec.org
http://www.spec.org/
## Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4650 v3, 2.10 GHz)

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<tr>
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</tr>
</thead>
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</tr>
<tr>
<td></td>
<td>Software Availability:</td>
<td>Nov-2014</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags (Continued)

- 429.mcf: basepeak = yes
  - `xCORE-AVX2(pass 2) -prof-gen(pass 1) -prof-use(pass 2)
    - ansi-alias -opt-mem-layout-trans=3`
- 445.gobmk: `xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32`
- 456.hmmer: `xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32`
- 458.sjeng: `xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll4 -auto-ilp32`
- 462.libquantum: basepeak = yes
- 464.h264ref: `xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -unroll4 -ansi-alias`

### C++ benchmarks:

- 471.omnetpp: `xCORE-AVX2(pass 2) -prof-gen(pass 1) -ipo(pass 2)
  -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)
  -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs
  -L/sh -lsmartheap`
- 473.astar: basepeak = yes
- 483.xalancbmk: basepeak = yes

### Peak Other Flags

- 403.gcc: `-Dalloca=_alloca`

The flags files that were used to format this result can be browsed at:

- [http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html](http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.html)

You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml](http://www.spec.org/cpu2006/flags/Intel-ic15.0-official-linux64.xml)
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For other inquiries, please contact webmaster@spec.org.

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