Non-Compliant

Huawei RH2288H V3 (Intel Xeon E5-2609 v4)

CPU2006 license: 3175
Test sponsor: Huawei
Tested by: Huawei
CPU Name: Intel Xeon E5-2609 v4

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the memory was not available as required by <a href="http://spec.org/cpu2006/Docs/runrules.html#rule_1.3.2">SPEC CPU rule 1.3.2</a> and the SPEC Open Systems Group policy on <a href="https://www.spec.org/osg/policy.html#AppendixC">general availability</a>.

### Hardware

<table>
<thead>
<tr>
<th>Copies</th>
<th>Operating System: Red Hat Enterprise Linux Server release 7.0 (Maipo) 3.10.0-123.el7.x86_64</th>
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<tbody>
<tr>
<td>400.perlbench</td>
<td>CPU: Intel Xeon E5-2609 v4</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>CPU Characteristics:</td>
</tr>
<tr>
<td>403.gcc</td>
<td>CPU MHz: 1700</td>
</tr>
<tr>
<td>429.mcf</td>
<td>FPU: Integrated</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>CPU(s) enabled: 16 cores, 2 chips, 8 cores/chip</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>CPU(s) orderable: 1,2 chip</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
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<tr>
<td>462.libquantum</td>
<td>Secondary Cache: 256 KB I+D on chip per core</td>
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<tr>
<td>464.h264ref</td>
<td>L3 Cache: 20 MB I+D on chip per chip</td>
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<tr>
<td>471.omnetpp</td>
<td>Other Cache: None</td>
</tr>
<tr>
<td>473.astar</td>
<td>Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2400T-R, running at 1866 MHz)</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>Disk Subsystem: 1 x 2 T SATA, 7200 RPM</td>
</tr>
</tbody>
</table>

### Software

| Operating System: Red Hat Enterprise Linux Server release 7.0 (Maipo) 3.10.0-123.el7.x86_64 |
|-----------|--------------------------------------------------------------------------------------------------|
| Compiler: C/C++: Version 16.0.0.101 of Intel C++ Studio XE for Linux |
| Auto Parallel: No |
| File System: ext4 |
| System State: Run level 3 (multi-user) |
| Base Pointers: 32-bit |
| Peak Pointers: 32/64-bit |
| Other Software: Microquill SmartHeap V10.2 |
Huawei RH2288H V3 (Intel Xeon E5-2609 v4)

**SPECint_rate2006 = NC**

**SPECint_rate_base2006 = NC**

**CPU2006 license:** 3175

**Test sponsor:** Huawei

**Test date:** Mar-2016

**Hardware Availability:** Mar-2016

**Tested by:** Huawei

**Software Availability:** Mar-2016

**Other Hardware:** None

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### Results Table

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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

BIOS configuration:
- Set Power Efficiency Mode to Performance
- Set Snoop Mode to ES mode
- Set Patrol Scrub to Disable

Sysinfo program /speccpu/spec16/config/sysinfo.rev6914

$Rev: 6914 $ $Date:: 2014-06-25 #$ e3fbb8667b5a285932ceab81e28219e1

running on localhost.localdomain Mon Mar 7 05:25:04 2016

Continued on next page
Huawei RH2288H V3 (Intel Xeon E5-2609 v4)

SPECint_rate2006 = NC
SPECint_rate_base2006 = NC

CPU2006 license: 3175
Test sponsor: Huawei
Test date: Mar-2016
Tested by: Huawei
Hardware Availability: Mar-2016
Software Availability: Mar-2016

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Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-2609 v4 @ 1.70GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7
cache size : 20480 KB

From /proc/meminfo
MemTotal:       263571176 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
NAME="Red Hat Enterprise Linux Server"
VERSION="7.0 (Maipo)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="7.0"
PRETTY_NAME="Red Hat Enterprise Linux Server 7.0 (Maipo)"
ANSI_COLOR="0;31"
CPE_NAME="cpe:/o:redhat:enterprise_linux:7.0:GA:server"
redhat-release: Red Hat Enterprise Linux Server release 7.0 (Maipo)
system-release: Red Hat Enterprise Linux Server release 7.0 (Maipo)
system-cpe: cpe:/o:redhat:enterprise_linux:7.0:ga:server
uname -a:
Linux localhost.localdomain 3.10.0-123.el7.x86_64 #1 SMP Mon May 5 11:16:57 EDT 2014 x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Mar 7 05:24
SPEC is set to: /speccpu/spec16

Continued on next page
Huawei
Huawei RH2288H V3 (Intel Xeon E5-2609 v4)

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Platform Notes (Continued)
Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Insyde Corp. 3.09 02/22/2016
Memory:
8x NO DIMM NO DIMM 3 rank
8x Samsung M393A2G40EB1-CRC 16 GB 1 rank 2400 MHz, configured at 1867 MHz
8x Samsung M393A2G40EB1-CRC 16 GB 2 rank 2400 MHz, configured at 1867 MHz

General Notes
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/speccpu/spec16/libs/32:/speccpu/spec16/libs/64:/speccpu/spec16/sh"

Binsaries compiled on a system with 1x Intel Core i5-4670K CPU + 32GB memory using RedHat EL 7.1
Transparent huge pages enabled with:
echo always >/sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1>/proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.: numactl --interleave=all runspec <etc>

Base Compiler Invocation
C benchmarks:
icc -m32 -L/opt/intelcompilers_and_libraries_2016/linux/compiler/lib/ia32_lin
C++ benchmarks:
icpc -m32 -L/opt/intelcompilers_and_libraries_2016/linux/compiler/lib/ia32_lin
Huawei RH2288H V3 (Intel Xeon E5-2609 v4)

CPU2006 license: 3175  
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---

**Base Portability Flags**

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX -IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

**Base Optimization Flags**

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch  
-opt-mem-layout-trans=5

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch  
-opt-mem-layout-trans=5 -Wl,-z,muldefs -L/sh -lsmartheap

**Base Other Flags**

C benchmarks:
-DALLOC=_alloca

**Peak Compiler Invocation**

C benchmarks (except as noted below):
icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

400.perlbench: icc -m64

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Non-Compliant
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Peak Compiler Invocation (Continued)

401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

Peak Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
458.sjeng: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -par-num-threads=1(pass 1) -prof-use(pass 2) -auto-ilp32

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -par-num-threads=1(pass 1) -prof-use(pass 2) -opt-prefetch -auto-ilp32 -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div
Huawei RH2288H V3 (Intel Xeon E5-2609 v4)

<table>
<thead>
<tr>
<th>SPECint_rate2006</th>
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### Peak Optimization Flags (Continued)

**C benchmarks:**

- 471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
- -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
- -par-num-threads=1(pass 1) -prof-use(pass 2) -unroll12
- -ansi-alias
- -opt-mem-layout-trans=3

**C++ benchmarks:**

- 471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen:threadsafe(pass 1)
- -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
- -par-num-threads=1(pass 1) -prof-use(pass 2) -unroll12
- -ansi-alias
- -opt-mem-layout-trans=3

### Peak Other Flags

**C benchmarks:**

- 403.gcc: -Dalloca=_alloca
Huawei RH2288H V3 (Intel Xeon E5-2609 v4)

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The flags files that were used to format this result can be browsed at:
- [Intel-ic16.0-official-linux64.html](http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.html)
- [Huawei-Platform-Settings-BDW-V1.0.html](http://www.spec.org/cpu2006/flags/Huawei-Platform-Settings-BDW-V1.0.html)

You can also download the XML flags sources by saving the following links:
- [Intel-ic16.0-official-linux64.xml](http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.xml)
- [Huawei-Platform-Settings-BDW-V1.0.xml](http://www.spec.org/cpu2006/flags/Huawei-Platform-Settings-BDW-V1.0.xml)

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For other inquiries, please contact webmaster@spec.org.

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