Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2699A v4 2.40 GHz)

SPECint\textsubscript{rate\_2006} = 1870
SPECint\textsubscript{rate\_base\_2006} = 1810

CPU\textsubscript{2006} license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

CPU Name: Intel Xeon E5-2699A v4
CPU Characteristics: Intel Turbo Boost Technology up to 3.60 GHz
CPU MHz: 2400
FPU: Integrated
CPU(s) enabled: 44 cores, 2 chips, 22 cores/chip, 2 threads/core
CPU(s) orderable: 1,2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 55 MB I+D on chip per chip
Other Cache: None
Memory: 256 GB (16 x 16 GB 2Rx4 PC4-2400T-R)
Disk Subsystem: 1 x 1.2 TB SAS HDD 10K RPM
Other Hardware: None

Software
Operating System: SUSE Linux Enterprise Server 12 SP1 (x86\textsubscript{64}) 3.12.49-11-default
Compiler: C/C++: Version 17.0.0.098 of Intel C/C++ Compiler for Linux
Auto Parallel: No
File System: xfs
System State: Run level 5 (multi-user)
Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2

SPEC\textsubscript{int\_rate\_2006} = 1870
SPEC\textsubscript{int\_rate\_base\_2006} = 1810
**Cisco Systems**

Cisco UCS C240 M4 (Intel Xeon E5-2699A v4 2.40 GHz)

**SPECint_rate2006 =** 1870

**SPECint_rate_base2006 =** 1810

---

**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<tbody>
<tr>
<td>400.perlbench</td>
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<td>554</td>
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<td>475</td>
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<td>475</td>
<td>1810</td>
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<tr>
<td>401.bzip2</td>
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<td>899</td>
<td>945</td>
<td>900</td>
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<td>897</td>
<td>949</td>
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<td>864</td>
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<tr>
<td>403.gcc</td>
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<td>429.mcf</td>
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<td>379</td>
<td>2110</td>
<td>382</td>
<td>2100</td>
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<td>445.gobmk</td>
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<td>456.hmmer</td>
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<tr>
<td>458.sjeng</td>
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<tr>
<td>462.libquantum</td>
<td>88</td>
<td>90.5</td>
<td>20200</td>
<td>90.4</td>
<td>20200</td>
<td>90.3</td>
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<td>90.3</td>
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</tr>
<tr>
<td>464.h264ref</td>
<td>88</td>
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<td>829</td>
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<td>824</td>
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<tr>
<td>471.omnetpp</td>
<td>88</td>
<td>683</td>
<td>805</td>
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<td>683</td>
<td>805</td>
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<tr>
<td>473.astar</td>
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<td>975</td>
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<tr>
<td>483.xalancbmk</td>
<td>88</td>
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<td>1690</td>
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<td>1690</td>
<td>357</td>
<td>1700</td>
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<td>358</td>
<td>1690</td>
<td>359</td>
<td>1690</td>
<td>357</td>
<td>1700</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

---

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

---

**Platform Notes**

BIOS Settings:
- CPU performance set to Enterprise
- Power Technology set to Performance
- Energy Performance BIAS setting set to Balanced Performance
- Memory RAS configuration set to Maximum Performance
- Memory Power Saving Mode set to Disabled
- QPI Snoop Mode set to Cluster-on-Die

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-cd5x Tue Jan 31 09:03:59 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) CPU E5-2699A v4 @ 2.40GHz
Continued on next page
Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2699A v4 2.40 GHz)
SPEClnt_rate2006 = 1870
SPEClnt_rate_base2006 = 1810

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

2 "physical id"s (chips)
88 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 22
siblings : 44
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 16 17 18 19 20 21 24 25 26 27 28

cache size : 28160 KB

From /proc/meminfo
   MemTotal:       264560428 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
   SUSE Linux Enterprise Server 12 SP1

From /etc/*release* /etc/*version*
   SuSE-release:
       SUSE Linux Enterprise Server 12 (x86_64)
       VERSION = 12
       PATCHLEVEL = 1
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
   os-release:
       NAME="SLES"
       VERSION="12-SP1"
       VERSION_ID="12.1"
       PRETTY_NAME="SUSE Linux Enterprise Server 12 SP1"
       ID="sles"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:12:sp1"

uname -a:
   Linux linux-cd5x 3.12.49-11-default #1 SMP Wed Nov 11 20:52:43 UTC 2015
   (8d714a0) x86_64 x86_64 x86_64 GNU/Linux

run-level 5 Jan 31 09:00

SPEC is set to: /opt/cpu2006-1.2

filesystem  type  size  used avail use% mounted on
/dev/sdai  xfs  1.1T  21G  1.1T  2% /

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to
SPEC CINT2006 Result

Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2699A v4 2.40 GHz)

SPECint_rate2006 = 1870
SPECint_rate_base2006 = 1810

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jan-2017
Hardware Availability: Apr-2016
Software Availability: Dec-2015

Platform Notes (Continued)

hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M4.2.0.13d.0.0812161132 08/12/2016
Memory:
16x 0xCE00 M393A2G40EB1-CRC 16 GB 2 rank 2400 MHz
8x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
echo 1> /proc/sys/vm/drop_caches
runcspec command invoked through numaclt i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Standard Performance Evaluation Corporation
info@spec.org
http://www.spec.org/
Cisco UCS C240 M4 (Intel Xeon E5-2699A v4 2.40 GHz)

**SPECint_rate2006 = 1870**

**SPECint_rate_base2006 = 1810**

CPU2006 license: 9019  
Test sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test date: Jan-2017  
Hardware Availability: Apr-2016  
Software Availability: Dec-2015

### Base Optimization Flags

C benchmarks:
- xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
- qopt-mem-layout-trans=3

C++ benchmarks:
- xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
- qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap

### Base Other Flags

C benchmarks:
- 403.gcc: -Dalloca=_alloca

### Peak Compiler Invocation

C benchmarks (except as noted below):
- `icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32`
  - 400.perlbench: `icc -m64`
  - 401.bzip2: `icc -m64`
  - 456.hmmer: `icc -m64`
  - 458.sjeng: `icc -m64`

C++ benchmarks:
- `icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32`

### Peak Portability Flags

400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
- 401.bzip2: `-DSPEC_CPU_LP64`
- 403.gcc: `-D_FILE_OFFSET_BITS=64`
- 429.mcf: `-D_FILE_OFFSET_BITS=64`
- 445.gobmk: `-D_FILE_OFFSET_BITS=64`
- 456.hmmer: `-DSPEC_CPU_LP64`
- 458.sjeng: `-DSPEC_CPU_LP64`
- 462.libquantum: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`
- 464.h264ref: `-D_FILE_OFFSET_BITS=64`
- 471.omnetpp: `-D_FILE_OFFSET_BITS=64`
- 473.astar: `-D_FILE_OFFSET_BITS=64`

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Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2699A v4 2.40 GHz)

SPECint_rate2006 = 1870
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Jan-2017
Hardware Availability: Apr-2016
Software Availability: Dec-2015

Peak Portability Flags (Continued)
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench:
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

401.bzip2:
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
-qopt-mem-layout-trans=3

403.gcc:
-xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3

429.mcf:
basepeak = yes

445.gobmk:
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-mem-layout-trans=3

456.hmmer:
-xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
-qopt-mem-layout-trans=3

458.sjeng:
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -auto-ilp32
-qopt-mem-layout-trans=3

462.libquantum:
basepeak = yes

464.h264ref:
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

C++ benchmarks:

471.omnetpp:
-prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2)
-qopt-ra-region-strategy=block
-qopt-mem-layout-trans=3 -Wl,-z,muldefs
-L/sh10.2 -lsmartheap

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Cisco Systems
Cisco UCS C240 M4 (Intel Xeon E5-2699A v4 2.40 GHz)

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Software Availability: Dec-2015

Peak Optimization Flags (Continued)

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revE.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revE.xml

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