Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4610 v4 1.80 GHz)

SPECint®2006 = 39.4
SPECint_base2006 = 37.9

Hardware
CPU Name: Intel Xeon E5-4610 v4
CPU Characteristics: 1800
FPU: Integrated
CPU(s) enabled: 40 cores, 4 chips, 10 cores/chip
CPU(s) orderable: 2.4 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 256 KB I+D on chip per core
L3 Cache: 25 MB I+D on chip per chip
Other Cache: None
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-2400T-R, running at 1866 MHz)
Disk Subsystem: 1 x 300 GB SAS, 15K RPM
Other Hardware: None

Software
Operating System: SUSE Linux Enterprise Server 12 SP1 (x86_64) 3.12.49-11-default
Compiler: C/C++: Version 16.0.0.101 of Intel C++ Studio XE for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2
## SPEC CINT2006 Result

### Cisco Systems

Cisco UCS B420 M4 (Intel Xeon E5-4610 v4 1.80 GHz)

**SPECint2006 = 39.4**  
**SPECint_base2006 = 37.9**

<table>
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<tr>
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<td>45.7</td>
<td>151</td>
<td>45.7</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The config file option 'submit' was used.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

BIOS Settings:
Intel Hyper-Threading Technology option set to Disabled
CPU performance set to Enterprise
Power Technology set to Energy Efficient
Energy Performance set to Balanced Performance
Memory RAS configuration set to Maximum Performance
Memory Power Saving Mode set to Disabled
QPI Snoop Mode set to Home Directory Snoop with OSB
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6914
$Rev: 6914 $ $Date:: 2014-06-25 $$ e3fbb8667b5a285932ceab81e28219e1
running on linux-1fno Fri Sep 2 11:10:36 2016

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E5-4610 v4 @ 1.80GHz
4 "physical id"s (chips)
Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4610 v4 1.80 GHz)

SPECint2006 = 39.4
SPECint_base2006 = 37.9

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Sep-2016
Hardware Availability: Jun-2016
Software Availability: Sep-2016

Platform Notes (Continued)

40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
  cpu cores : 10
  siblings : 10
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12
  physical 2: cores 0 1 2 3 4 8 9 10 11 12
  physical 3: cores 0 1 2 3 4 8 9 10 11 12
  cache size : 25600 KB

From /proc/meminfo
  MemTotal: 529169068 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 1
  # This file is deprecated and will be removed in a future service pack or
  # release.
  # Please check /etc/os-release for details about this release.
  os-release:
  NAME="SLES"
  VERSION="12-SP1"
  VERSION_ID="12.1"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP1"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp1"

  uname -a:
  (8d714a0) x86_64 x86_64 x86_64 GNU/Linux

  run-level 3 Sep 1 10:31

  SPEC is set to: /opt/cpu2006-1.2

  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda1 xfs 280G 14G 266G 5% /

  Additional information from dmidecode:

  Warning: Use caution when you interpret this section. The 'dmidecode' program
  reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
  hardware, firmware, and the "DMTF SMBIOS" standard.

  BIOS Cisco Systems, Inc. B420M4.3.1.2d.0.081120161622 08/11/2016
  Memory:

Continued on next page
Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4610 v4 1.80 GHz)

| SPECint2006  | 39.4 |
| SPECint_base2006 | 37.9 |

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)
32x 0xAD00 HMA42GR7AFR4N-UH 16 GB 2 rank 2400 MHz, configured at 1866 MHz
16x NO DIMM NO DIMM

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact,1,0"
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"
OMP_NUM_THREADS = "40"

Binaries compiled on a system with 1x Intel Core i5-4670K CPU + 32GB memory using RedHat EL 7.1
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
  icc -m64

C++ benchmarks
  icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
  -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -opt-prefetch -auto-p32

Continued on next page
**Cisco Systems**  
Cisco UCS B420 M4 (Intel Xeon E5-4610 v4 1.80 GHz)  

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<td>Test date: Sep-2016</td>
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<tr>
<td>Test sponsor: Cisco Systems</td>
<td>Hardware Availability: Jun-2016</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Sep-2016</td>
</tr>
</tbody>
</table>

**Base Optimization Flags (Continued)**

-xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch -auto-p32
-W1,-z,muldefs -L/sh -lsmartheap64

**Base Other Flags**

C benchmarks:
403.gcc: -Dalloca=_alloca

**Peak Compiler Invocation**

C benchmarks (except as noted below):
icc -m64

400.perlbench: icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
445.gobmk: icc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):
icpc -m32 -L/opt/intel/compilers_and_libraries_2016/linux/compiler/lib/ia32_lin
473.astar: icpc -m64

**Peak Portability Flags**

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
Cisco Systems
Cisco UCS B420 M4 (Intel Xeon E5-4610 v4 1.80 GHz)

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SPECint_base2006 = 37.9

CPU2006 license: 9019  Test date: Sep-2016
Test sponsor: Cisco Systems  Hardware Availability: Jun-2016
Tested by: Cisco Systems  Software Availability: Sep-2016

Peak Optimization Flags

C benchmarks:

400.perlbench: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
  -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
  -par-num-threads=1(pass 1) -prof-use(pass 2) -opt-prefetch
  -ansi-alias

401.bzip2: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
  -ipo(pass 2) -O3(pass 2) -no-prec-div
  -par-num-threads=1(pass 1) -prof-use(pass 2) -auto-ilp32
  -opt-prefetch -ansi-alias

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div -inline-calloc
  -opt-malloc-options=3 -auto-ilp32

429.mcf: -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
  -opt-prefetch -auto-p32

445.gobmk: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
  -prof-use(pass 2) -par-num-threads=1(pass 1) -ansi-alias

456.hmmer: basepeak = yes

458.sjeng: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
  -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
  -par-num-threads=1(pass 1) -prof-use(pass 2) -unroll4

462.libquantum: basepeak = yes

464.h264ref: basepeak = yes

C++ benchmarks:

471.omnetpp: -xCORE-AVX2(pass 2) -prof-gen:threadsafepass 1
  -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2)
  -par-num-threads=1(pass 1) -prof-use(pass 2)
  -opt-ra-region-strategy=block -ansi-alias
  -Wl,-z,muldefs -L/sh -lsmartheap

473.astar: -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
  -auto-p32 -Wl,-z,muldefs -L/sh -lsmartheap64

483.xalancbmk: -xCORE-AVX2 -ipo -O3 -no-prec-div -opt-prefetch
  -ansi-alias -Wl,-z,muldefs -L/sh -lsmartheap
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Peak Other Flags

C benchmarks:

403.gcc -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revE.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic16.0-official-linux64.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revE.xml

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