Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6138, 2.00GHz)

SPECfp®2006 = 145
SPECfp_base2006 = 137

Hardware
CPU Name: Intel Xeon Gold 6138
CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
CPU MHz: 2000
FPU: Integrated
CPU(s) enabled: 40 cores, 2 chips, 20 cores/chip
CPU(s) orderable: 1.2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core

Software
Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)

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Cisco Systems
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SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
L3 Cache: 27.5 MB I+D on chip per chip
Other Cache: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 300 GB SAS 10K RPM
Other Hardware: None
Base Pointers: 64-bit
Peak Pointers: 32/64-bit

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>13.8</td>
<td>983</td>
<td>14.0</td>
<td>971</td>
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<tr>
<td>416.gamess</td>
<td>410</td>
<td>47.8</td>
<td>409</td>
<td>47.9</td>
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<tr>
<td>433.milc</td>
<td>119</td>
<td>77.2</td>
<td>116</td>
<td>79.0</td>
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<tr>
<td>434.zeusmp</td>
<td>37.0</td>
<td>246</td>
<td>37.4</td>
<td>243</td>
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<td>435.gromacs</td>
<td>158</td>
<td>45.1</td>
<td>158</td>
<td>45.3</td>
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<tr>
<td>436.cactusADM</td>
<td>9.20</td>
<td>1300</td>
<td>9.09</td>
<td>1320</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>21.1</td>
<td>445</td>
<td>21.3</td>
<td>442</td>
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<tr>
<td>444.namd</td>
<td>225</td>
<td>35.6</td>
<td>225</td>
<td>35.6</td>
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<tr>
<td>447.dealII</td>
<td>157</td>
<td>72.8</td>
<td>157</td>
<td>72.9</td>
</tr>
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<td>450.soplex</td>
<td>160</td>
<td>52.0</td>
<td>160</td>
<td>52.2</td>
</tr>
<tr>
<td>453.povray</td>
<td>76.6</td>
<td>69.4</td>
<td>76.6</td>
<td>69.4</td>
</tr>
<tr>
<td>454.calculix</td>
<td>116</td>
<td>70.9</td>
<td>117</td>
<td>70.6</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>40.7</td>
<td>261</td>
<td>40.4</td>
<td>263</td>
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<tr>
<td>465.tonto</td>
<td>223</td>
<td>44.1</td>
<td>220</td>
<td>44.7</td>
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<tr>
<td>470.lbm</td>
<td>9.02</td>
<td>1520</td>
<td>9.00</td>
<td>1530</td>
</tr>
<tr>
<td>481.wrf</td>
<td>85.9</td>
<td>130</td>
<td>85.6</td>
<td>131</td>
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<tr>
<td>482.sphinx3</td>
<td>318</td>
<td>61.3</td>
<td>319</td>
<td>61.0</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-j64x Sun Aug 20 11:13:07 2017
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Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6138, 2.00GHz)

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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6138 CPU @ 2.00GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  cache size : 28160 KB

From /proc/meminfo
MemTotal: 394864840 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-j64x 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 20 11:01

SPEC is set to: /home/cpu2006-1.2

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb7 xfs 416G 19G 398G 5% /home
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6138, 2.00GHz)

SPECfp2006 = 145
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Aug-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "40"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
  icc -m64
C++ benchmarks:
  icpc -m64
Fortran benchmarks:
  ifort -m64
Benchmarks using both Fortran and C:
  icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main

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## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6138, 2.00GHz)

<table>
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### CPU2006 license: 9019
Test date: Aug-2017

Test sponsor: Cisco Systems
Software Availability: Apr-2017

Tested by: Cisco Systems
Hardware Availability: Aug-2017

### Base Portability Flags (Continued)

<table>
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<td><code>-DSPEC_CPU_LP64</code> <code>-nofor_main</code></td>
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<tr>
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<td><code>-DSPEC_CPU_LP64</code></td>
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<td><code>-DSPEC_CPU_LP64</code> <code>-nofor_main</code></td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td><code>-DSPEC_CPU_LP64</code> <code>-nofort_main</code></td>
</tr>
<tr>
<td>463.tonto</td>
<td><code>-DSPEC_CPU_LP64</code></td>
</tr>
<tr>
<td>470.lbm</td>
<td><code>-DSPEC_CPU_LP64</code></td>
</tr>
<tr>
<td>481.wrf</td>
<td><code>-DSPEC_CPU_LP64</code> <code>-DSPEC_CPU_CASE_FLAG</code> <code>-DSPEC_CPU_LINUX</code></td>
</tr>
<tr>
<td>482.sphinx3</td>
<td><code>-DSPEC_CPU_LP64</code></td>
</tr>
</tbody>
</table>

### Base Optimization Flags

- **C benchmarks:**
  `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-parallel` `-qopt-prefetch`

- **C++ benchmarks:**
  `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-qopt-prefetch`

- **Fortran benchmarks:**
  `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-parallel` `-qopt-prefetch`

- **Benchmarks using both Fortran and C:**
  `-xCORE-AVX2` `-ipo` `-O3` `-no-prec-div` `-parallel` `-qopt-prefetch`

### Peak Compiler Invocation

- **C benchmarks:**
  `icc -m64`

- **C++ benchmarks:**
  `icpc -m64`

- **Fortran benchmarks:**
  `ifort -m64`

- **Benchmarks using both Fortran and C:**
  `icc -m64 ifort -m64`
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6138, 2.00GHz)

SPECfp2006 = 145
SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Aug-2017
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:
444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -fno-alias -auto-ilp32

447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-

434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes
459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0
-qopt-prefetch -parallel

465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -inline-calloc -qopt-malloc-options=3
-auto -unroll4

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Peak Optimization Flags (Continued)

Benchmarks using both Fortran and C:

435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes
454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-ilp32
481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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