Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4114, 2.20GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
- CPU Name: Intel Xeon Silver 4114
- CPU Characteristics: Intel Turbo Boost Technology up to 3.00 GHz
- CPU MHz: 2200
- FPU: Integrated
- CPU(s) enabled: 20 cores, 2 chips, 10 cores/chip, 2 threads/core
- CPU(s) orderable: 1.2 chips
- Primary Cache: 32 KB I + 32 KB D on chip per core
- Secondary Cache: 1 MB I+D on chip per core
- L3 Cache: 13.75 MB I+D on chip per chip
- Other Cache: None
- Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400 MHz)
- Disk Subsystem: 1 x 800 GB SSD SAS
- Other Hardware: None

Software
- Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
- Auto Parallel: Yes
- File System: xfs
- System State: Run level 3 (multi-user)
- Base Pointers: 32-bit
- Peak Pointers: 32/64-bit
- Other Software: Microquill SmartHeap V10.2

SPECint®_rate2006 = 953
SPECint_rate_base2006 = 905
### Cisco Systems

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</table>

**Results Table**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Platform Notes**

BIOS Settings:
- Intel HyperThreading Technology set to Enabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- SNC set to Enabled
- IMC Interleaving set to 1-way Interleave
- Patrol Scrub set to Disabled
- Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993
- Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f9f8696cbe290c1)
- Running on linux-0s5q Sat Sep 2 17:00:34 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

model name: Intel(R) Xeon(R) Silver 4114 CPU @ 2.20GHz

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Platform Notes (Continued)

2 "physical id"s (chips)  
40 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The  
following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 10  
siblings : 20  
physical 0: cores 0 1 2 3 4 8 9 10 11 12  
physical 1: cores 0 1 2 3 4 8 9 10 11 12  
cache size : 14080 KB  

From /proc/meminfo  
MemTotal: 394864292 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB  

From /etc/*release*/etc/*version*  
SuSE-release:  
SUSE Linux Enterprise Server 12 (x86_64)  
VERSION = 12  
PATCHLEVEL = 2  
# This file is deprecated and will be removed in a future service pack or  
release.  
# Please check /etc/os-release for details about this release.  

os-release:  
NAME="SLES"  
VERSION="12-SP2"  
VERSION_ID="12.2"  
PATTERN=\"SUSE Linux Enterprise Server 12 SP2\"  
ID=sles  
ANSI_COLOR=\"0;32\"  
CPE_NAME=\"cpe:/o:suse:sles:12:sp2\"  

uname -a:  
Linux linux-0s5q 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016  
(9464f67) x86_64 x86_64 x86_64 GNU/Linux  
run-level 3 Sep 2 16:58  

SPEC is set to: /opt/cpu2006-1.2  

Filesystem Type Size Used Avail Use% Mounted on  
/dev/sdb2 xfs 700G 61G 640G 9% /  

Additional information from dmidecode:  

Warning: Use caution when you interpret this section. The 'dmidecode' program  
reads system data which is "intended to allow hardware to be accurately  
determined", but the intent may not be met, as there are frequent changes to  
hardware, firmware, and the "DMTF SMBIOS" standard.  

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017  
Memory:  
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz, configured at 2400 MHz  
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CPU2006 license: 9019
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Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib/ia32:/opt/cpu2006-1.2/lib/intel64:/opt/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3

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SPEC CINT2006 Result

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4114, 2.20GHz)

SPECint_rate2006 = 953
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CPU2006 license: 9019
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Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Base Optimization Flags (Continued)

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
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CPU2006 license: 9019
Test date: Sep-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

### Peak Optimization Flags

**C benchmarks:**

- 400.perlbench:
  -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

- 401.bzip2:
  -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
  -qopt-mem-layout-trans=3

- 403.gcc:
  -xCORE-AVX2 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=3

- 429.mcf: basepeak = yes

- 445.gobmk:
  -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -qopt-mem-layout-trans=3

- 456.hmmer:
  -xCORE-AVX2 -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
  -qopt-mem-layout-trans=3

- 458.sjeng:
  -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -unroll4 -auto-ilp32
  -qopt-mem-layout-trans=3

- 462.libquantum: basepeak = yes

- 464.h264ref:
  -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

**C++ benchmarks:**

- 471.omnetpp:
  -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2)
  -qopt-ra-region-strategy=block
  -qopt-mem-layout-trans=3 -Wl, -z, muldefs
  -L/sh10.2 -lsmartheap

- 473.astar: basepeak = yes

- 483.xalancbmk: basepeak = yes
# SPEC CINT2006 Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4114, 2.20GHz)

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### CPU2006 license: 9019

**Test date:** Sep-2017

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## Peak Other Flags

C benchmarks:

403.gcc -Dalloca=_alloca

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


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For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.


Originally published on 19 September 2017.