Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132 2.60GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2006 license: 9019</td>
<td>CPU Name: Intel Xeon Gold 6132</td>
</tr>
<tr>
<td>Test sponsor: Cisco Systems</td>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>CPU MHz: 2600</td>
</tr>
<tr>
<td>CPU Name: Intel Xeon Gold 6132</td>
<td>FPU: Integrated</td>
</tr>
<tr>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz</td>
<td>CPU(s) enabled: 56 cores, 4 chips, 14 cores/chip</td>
</tr>
<tr>
<td>CPU MHz: 2600</td>
<td>CPU(s) orderable: 2,4 chips</td>
</tr>
<tr>
<td>FPU: Integrated</td>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>CPU(s) enabled: 56 cores, 4 chips, 14 cores/chip</td>
<td>Secondary Cache: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>CPU(s) orderable: 2,4 chips</td>
<td>Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default</td>
</tr>
<tr>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
<td>Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux; Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Secondary Cache: 1 MB I+D on chip per core</td>
<td>Auto Parallel: Yes</td>
</tr>
<tr>
<td></td>
<td>File System: xfs</td>
</tr>
<tr>
<td></td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
</tbody>
</table>

SPECfp®2006 = 148
SPECfp_base2006 = 143
## SPEC CFP2006 Result

### Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6132 2.60GHz)

<table>
<thead>
<tr>
<th>CPU2006 license: 9019</th>
<th>Test date: Aug-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Apr-2017</td>
</tr>
</tbody>
</table>

L3 Cache: 19.25 MB I+D on chip per chip
Other Cache: None
Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 800 GB SAS SSD
Other Hardware: None

Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other Software: None

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base Pointers</th>
<th>Peak Pointers</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>410.bwaves</td>
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<td>73.7</td>
<td>265</td>
<td>73.7</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-nvug Thu Aug 31 02:33:36 2017
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Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132 2.60GHz)

SPECfp2006 = 148
SPECfp_base2006 = 143

CPU2006 license: 9019
Test date: Aug-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6132 CPU @ 2.60GHz
4 "physical id"s (chips)
56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 14
siblings : 14
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
cache size : 19712 KB

From /proc/meminfo
MemTotal: 791193276 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
(9464f67) x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Aug 31 02:14

SPEC is set to: /home/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 644G 96G 548G 15% /
Additional information from dmidecode:
Continued on next page
## SPEC CFP2006 Result

### Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132 2.60GHz)

| SPECfp2006 = | 148 |
| SPECfp_base2006 = | 143 |

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| Tested by: | Cisco Systems |
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### Platform Notes (Continued)

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017

Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

### General Notes

Environment variables set by runspec before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
- OMP_NUM_THREADS = "56"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2

Transparent Huge Pages enabled with:
- echo always > /sys/kernel/mm/transparent_hugepage/enabled

### Base Compiler Invocation

C benchmarks:
- icc -m64

C++ benchmarks:
- icpc -m64

Fortran benchmarks:
- ifort -m64

Benchmarks using both Fortran and C:
- icc -m64 ifort -m64

### Base Portability Flags

- 410.bwaves: -DSPEC_CPU_LP64
- 416.gamess: -DSPEC_CPU_LP64
- 433.milc: -DSPEC_CPU_LP64
- 434.zeusmp: -DSPEC_CPU_LP64
- 435.gromacs: -DSPEC_CPU_LP64 -nofor_main
- 436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
Cisco Systems
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Base Portability Flags (Continued)

437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -03 -no-prec-div -parallel -qopt-prefetch

C++ benchmarks:
-xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch

Fortran benchmarks:
-xCORE-AVX2 -ipo -03 -no-prec-div -parallel -qopt-prefetch

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -03 -no-prec-div -parallel -qopt-prefetch

Peak Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Peak Portability Flags
Same as Base Portability Flags
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6132 2.60GHz)

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SPECfp_base2006 = 143

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Aug-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags

C benchmarks:
- 433.milc: basepeak = yes
- 470.lbm: basepeak = yes
- 482.sphinx3: basepeak = yes

C++ benchmarks:
- 444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -fno-alias -auto-ilp32
- 447.dealII: basepeak = yes
- 450.soplex: basepeak = yes
- 453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
- 410.bwaves: basepeak = yes
- 416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-
- 434.zeusmp: basepeak = yes
- 437.leslie3d: basepeak = yes
- 459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -unroll2 -inline-level=0 -qopt-prefetch -parallel
- 465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -inline-calloc -qopt-malloc-options=3
  -auto -unroll4

Benchmarks using both Fortran and C:
- 435.gromacs: basepeak = yes
- 436.cactusADM: basepeak = yes

Continued on next page
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| CPU2006 license: 9019 | Test date: Aug-2017 |
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Peak Optimization Flags (Continued)

454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-ilp32

481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml