Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8156 3.60GHz)

SPECfp®2006 = 140
SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Platinum 8156
CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
CPU MHz: 3600
FPU: Integrated
CPU(s) enabled: 16 cores, 4 chips, 4 cores/chip
CPU(s) orderable: 2, 4 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core

Software
Operating System: SUSE Linux Enterprise Server 12 SP2
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 5 (multi-user)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8156 3.60GHz)

SPECfp2006 = 140
SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
L3 Cache: 16.5 MB I+D on chip per chip
Other Cache: None
Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 800 GB SAS SSD
Other Hardware: None
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other Software: None

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>Peak</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Seconds</td>
<td>Ratio</td>
<td>Seconds</td>
<td>Ratio</td>
<td>Seconds</td>
<td>Ratio</td>
<td>Seconds</td>
<td>Ratio</td>
<td></td>
</tr>
<tr>
<td>410.bwaves</td>
<td>11.4</td>
<td>1190</td>
<td>11.2</td>
<td>1210</td>
<td>11.2</td>
<td>1210</td>
<td>11.2</td>
<td>1210</td>
<td>11.2</td>
<td></td>
</tr>
<tr>
<td>416.gamess</td>
<td>399</td>
<td>49.1</td>
<td>399</td>
<td>49.1</td>
<td>399</td>
<td>49.1</td>
<td>378</td>
<td>51.7</td>
<td>381</td>
<td>51.4</td>
</tr>
<tr>
<td>433.milc</td>
<td>122</td>
<td>75.2</td>
<td>121</td>
<td>75.9</td>
<td>122</td>
<td>75.1</td>
<td>122</td>
<td>75.2</td>
<td>121</td>
<td>75.9</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>44.9</td>
<td>203</td>
<td>44.8</td>
<td>203</td>
<td>43.2</td>
<td>210</td>
<td>44.9</td>
<td>203</td>
<td>44.8</td>
<td>203</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>104</td>
<td>68.9</td>
<td>104</td>
<td>68.9</td>
<td>104</td>
<td>69.0</td>
<td>104</td>
<td>68.9</td>
<td>104</td>
<td>69.0</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>11.4</td>
<td>1050</td>
<td>11.5</td>
<td>1040</td>
<td>11.5</td>
<td>1040</td>
<td>11.5</td>
<td>1040</td>
<td>11.5</td>
<td>1040</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>18.4</td>
<td>512</td>
<td>19.4</td>
<td>483</td>
<td>18.9</td>
<td>497</td>
<td>18.4</td>
<td>512</td>
<td>19.4</td>
<td>483</td>
</tr>
<tr>
<td>444.namd</td>
<td>225</td>
<td>35.7</td>
<td>225</td>
<td>35.7</td>
<td>225</td>
<td>35.7</td>
<td>219</td>
<td>36.6</td>
<td>219</td>
<td>36.6</td>
</tr>
<tr>
<td>447.dealII</td>
<td>158</td>
<td>72.2</td>
<td>159</td>
<td>72.1</td>
<td>159</td>
<td>71.9</td>
<td>158</td>
<td>72.2</td>
<td>159</td>
<td>72.1</td>
</tr>
<tr>
<td>450.soplex</td>
<td>173</td>
<td>48.1</td>
<td>171</td>
<td>48.7</td>
<td>172</td>
<td>48.6</td>
<td>173</td>
<td>48.1</td>
<td>171</td>
<td>48.7</td>
</tr>
<tr>
<td>453.povray</td>
<td>76.4</td>
<td>69.7</td>
<td>76.1</td>
<td>69.9</td>
<td>76.1</td>
<td>69.9</td>
<td>67.4</td>
<td>78.9</td>
<td>67.2</td>
<td>79.2</td>
</tr>
<tr>
<td>454.calculix</td>
<td>108</td>
<td>76.1</td>
<td>108</td>
<td>76.2</td>
<td>108</td>
<td>76.1</td>
<td>108</td>
<td>76.5</td>
<td>108</td>
<td>76.5</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>54.3</td>
<td>195</td>
<td>51.7</td>
<td>205</td>
<td>57.2</td>
<td>186</td>
<td>51.1</td>
<td>208</td>
<td>56.9</td>
<td>187</td>
</tr>
<tr>
<td>465.tonto</td>
<td>167</td>
<td>58.9</td>
<td>171</td>
<td>57.7</td>
<td>169</td>
<td>58.2</td>
<td>148</td>
<td>66.5</td>
<td>148</td>
<td>66.6</td>
</tr>
<tr>
<td>470.lbm</td>
<td>11.8</td>
<td>1160</td>
<td>11.9</td>
<td>1150</td>
<td>11.9</td>
<td>1150</td>
<td>11.8</td>
<td>1160</td>
<td>11.9</td>
<td>1150</td>
</tr>
<tr>
<td>481.wrf</td>
<td>121</td>
<td>92.0</td>
<td>120</td>
<td>93.0</td>
<td>120</td>
<td>93.4</td>
<td>121</td>
<td>92.0</td>
<td>120</td>
<td>93.0</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>232</td>
<td>84.1</td>
<td>233</td>
<td>83.6</td>
<td>232</td>
<td>83.8</td>
<td>232</td>
<td>84.1</td>
<td>233</td>
<td>83.6</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-g4f1Fri Aug 25 08:51:46 2017
Continued on next page
Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
   http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Platinum 8156 CPU @ 3.60GHz
   4 "physical id"s (chips)
   16 "processors"
   cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
   cpu cores : 4
   siblings : 4
   physical 0: cores 1 5 9 13
   physical 1: cores 0 5 9 13
   physical 2: cores 3 4 6 7
   physical 3: cores 1 5 9 13
   cache size : 16896 KB

From /proc/meminfo
   MemTotal:       790968724 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
   SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
   SuSE-release:
      SUSE Linux Enterprise Server 12 (x86_64)
      VERSION = 12
      PATCHLEVEL = 2
      # This file is deprecated and will be removed in a future service pack or release.
      # Please check /etc/os-release for details about this release.
   os-release:
      NAME="SLES"
      VERSION="12-SP2"
      VERSION_ID="12.2"
      PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
      ID="sles"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
   Linux linux-g4f1 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
      (9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 5 Aug 25 08:48

SPEC is set to: /home/cpu2006-1.2
Cisco UCS C480 M5 (Intel Xeon Platinum 8156 3.60GHz)

SPECfp2006 = 140
SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

Filesystem     Type  Size  Used  Avail  Use%  Mounted on
/dev/sda6      xfs   871G   35G  837G   4%   /home

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(Base of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "~/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "16"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: −DSPEC_CPU_LP64
416.gamess: −DSPEC_CPU_LP64
433.milc: −DSPEC_CPU_LP64

Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8156 3.60GHz)

SPECfp2006 = 140
SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Aug-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Base Portability Flags (Continued)

- 434.zeusmp: -DSPEC_CPU_LP64
- 435.gromacs: -DSPEC_CPU_LP64 -nofor_main
- 436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
- 437.leslie3d: -DSPEC_CPU_LP64
- 444.namd: -DSPEC_CPU_LP64
- 447.dealII: -DSPEC_CPU_LP64
- 450.soplex: -DSPEC_CPU_LP64
- 453.povray: -DSPEC_CPU_LP64
- 454.calculix: -DSPEC_CPU_LP64 -nofor_main
- 459.GemsFDTD: -DSPEC_CPU_LP64
- 465.tonto: -DSPEC_CPU_LP64
- 481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
- 482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Peak Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8156 3.60GHz)

SPECfp2006 = 140
SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Aug-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:
444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -fno-alias -auto-iipt32
447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-
434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes
459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -qopt-prefetch -parallel
465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -inline-calloc -qopt-malloc-options=3
-auto -unroll4

Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Platinum 8156 3.60GHz)

SPECfp2006 = 140
SPECfp_base2006 = 137

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Aug-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags (Continued)

Benchmarks using both Fortran and C:

435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes
454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-ilp32
481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC and SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Originally published on 19 September 2017.