## SPEC® CINT2006 Result

**Cisco Systems**

Cisco UCS C480 M5 (Intel Xeon Gold 6140M, 2.30GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Operating System: SUSE Linux Enterprise Server 12 SP2 (x86-64) 4.4.21-69-default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux</td>
<td></td>
</tr>
<tr>
<td>Auto Parallel: Yes</td>
<td></td>
</tr>
<tr>
<td>File System: xfs</td>
<td></td>
</tr>
<tr>
<td>System State: Run level 5 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers: 32-bit</td>
<td></td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td></td>
</tr>
<tr>
<td>Other Software: Microquill SmartHeap V10.2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hardware</th>
<th>CPU Name: Intel Xeon Gold 6140M</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz</td>
<td></td>
</tr>
<tr>
<td>CPU MHz: 2300</td>
<td></td>
</tr>
<tr>
<td>FPU: Integrated</td>
<td></td>
</tr>
<tr>
<td>CPU(s) enabled: 72 cores, 4 chips, 18 cores/chip, 2 threads/core</td>
<td></td>
</tr>
<tr>
<td>CPU(s) orderable: 2,4 chips</td>
<td></td>
</tr>
<tr>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
<td></td>
</tr>
<tr>
<td>Secondary Cache: 1 MB I+D on chip per core</td>
<td></td>
</tr>
<tr>
<td>L3 Cache: 24.75 MB I+D on chip per chip</td>
<td></td>
</tr>
<tr>
<td>Other Cache: None</td>
<td></td>
</tr>
<tr>
<td>Memory: 768 GB (4x 16 GB 2Rx4 PC4-2666V-R)</td>
<td></td>
</tr>
<tr>
<td>Disk Subsystem: 1 x 1 TB SAS HDD, 7.2K RPM</td>
<td></td>
</tr>
<tr>
<td>Other Hardware: None</td>
<td></td>
</tr>
</tbody>
</table>

### SPECint Rate 2006

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECint_rate2006</th>
<th>SPECint_rate_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>3750</td>
<td>3500</td>
</tr>
<tr>
<td>bzip2</td>
<td>3750</td>
<td>3500</td>
</tr>
<tr>
<td>gcc</td>
<td>2540</td>
<td>2300</td>
</tr>
<tr>
<td>mcf</td>
<td>4810</td>
<td>4580</td>
</tr>
<tr>
<td>gobmk</td>
<td>2090</td>
<td>2000</td>
</tr>
<tr>
<td>hammer</td>
<td>5680</td>
<td>5460</td>
</tr>
<tr>
<td>sjeng</td>
<td>4200</td>
<td>4000</td>
</tr>
<tr>
<td>libquantum</td>
<td>2510</td>
<td>2420</td>
</tr>
<tr>
<td>h264ref</td>
<td>3960</td>
<td>3800</td>
</tr>
<tr>
<td>omnetpp</td>
<td>1970</td>
<td>1830</td>
</tr>
<tr>
<td>astar</td>
<td>2250</td>
<td>2150</td>
</tr>
<tr>
<td>xalancbmk</td>
<td>4000</td>
<td>3800</td>
</tr>
</tbody>
</table>

| CPU2006 license: 9019 |
| Test sponsor: Cisco Systems |
| Tested by: Cisco Systems |
| Test date: Sep-2017 |
| Hardware Availability: Aug-2017 |
| Software Availability: Apr-2017 |
## SPEC CINT2006 Result

### Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6140M, 2.30GHz)

| SPECint_rate2006 | 3680 |
| SPECint_rate_base2006 | 3500 |

**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

- **Test date:** Sep-2017  
- **Hardware Availability:** Aug-2017  
- **Software Availability:** Apr-2017

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds - Base</th>
<th>Ratio</th>
<th>Seconds - Peak</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>144</td>
<td>545 &amp; 2580</td>
<td>545 &amp; 2580</td>
<td>544 &amp; 2590</td>
<td>544 &amp; 2590</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>144</td>
<td>463 &amp; 2510</td>
<td>465 &amp; 2490</td>
<td>462 &amp; 2510</td>
<td>461 &amp; 2510</td>
</tr>
<tr>
<td>403.gcc</td>
<td>144</td>
<td>273 &amp; 4810</td>
<td>273 &amp; 4810</td>
<td>273 &amp; 4810</td>
<td>273 &amp; 4810</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>144</td>
<td>720 &amp; 2250</td>
<td>724 &amp; 2250</td>
<td>724 &amp; 2250</td>
<td>724 &amp; 2250</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>144</td>
<td>52.9 &amp; 55600</td>
<td>52.9 &amp; 55600</td>
<td>52.9 &amp; 55600</td>
<td>52.9 &amp; 55600</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>144</td>
<td>838 &amp; 3820</td>
<td>836 &amp; 3810</td>
<td>836 &amp; 3810</td>
<td>836 &amp; 3810</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>144</td>
<td>249 &amp; 4000</td>
<td>248 &amp; 4000</td>
<td>248 &amp; 4000</td>
<td>248 &amp; 4000</td>
</tr>
</tbody>
</table>

**Notes:**
- Results appear in the order in which they were run. Bold underlined text indicates a median measurement.
- The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
- For details, please see the config file.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Enabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS
  - SNC set to Enabled
  - IMC Interleaving set to 1-way Interleave
  - Patrol Scrub set to Disabled

- **Sysinfo program** /home/cpu2006-1.2/config/sysinfo.rev6993
- **Revision** 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
- **Running on** linux-g4f1 Mon Sep 11 18:36:59 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo

- **model name:** Intel(R) Xeon(R) Gold 6140M CPU @ 2.30GHz

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Platform Notes (Continued)

4 "physical id"s (chips)
144 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 36
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
cache size : 25344 KB

From /proc/meminfo
MemTotal: 790967132 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SUSE-release:
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

uname -a:
Linux linux-g4f1 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 5 Oct 11 14:12

SPEC is set to: /home/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda6 xfs 871G 35G 836G 4% /home

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to...
Cisco Systems
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CPU2006 license: 9019
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Platform Notes (Continued)

hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "~/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transient_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runcspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
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**Base Optimization Flags**

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/sh10.2 -lsmartheap

**Base Other Flags**

C benchmarks:
403.gcc: -Dallocation=-alloca

**Peak Compiler Invocation**

C benchmarks (except as noted below):
`icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32`

400.perlbench: `icc -m64`
401.bzip2: `icc -m64`
456.hmmer: `icc -m64`
458.sjeng: `icc -m64`

C++ benchmarks:
`icpc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32`

**Peak Portability Flags**

400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
401.bzip2: `-DSPEC_CPU_LP64`
403.gcc: `-D_FILE_OFFSET_BITS=64`
429.mcf: `-D_FILE_OFFSET_BITS=64`
445.gobmk: `-D_FILE_OFFSET_BITS=64`
456.hmmer: `-DSPEC_CPU_LP64`
458.sjeng: `-DSPEC_CPU_LP64`
462.libquantum: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`
464.h264ref: `-D_FILE_OFFSET_BITS=64`
471.omnetpp: `-D_FILE_OFFSET_BITS=64`
473.astar: `-D_FILE_OFFSET_BITS=64`
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Peak Portability Flags (Continued)
483.xalancbmk: -D_FILE_OFFSET_BITS=64  -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:
400.perlbench: -prof-gen(pass 1)  -prof-use(pass 2)  -xCORE-AVX512(pass 2)
 -par-num-threads=1(pass 1)  -ipo(pass 2)  -O3(pass 2)
 -no-prec-div(pass 2)  -auto-ilp32  -qopt-mem-layout-trans=3

401.bzip2: -prof-gen(pass 1)  -prof-use(pass 2)  -xCORE-AVX512(pass 2)
 -par-num-threads=1(pass 1)  -ipo(pass 2)  -O3(pass 2)
 -no-prec-div(pass 2)  -qopt-prefetch  -auto-ilp32
 -qopt-mem-layout-trans=3

403.gcc: -xCORE-AVX512  -ipo  -O3  -no-prec-div
 -qopt-mem-layout-trans=3

429.mcf: basepeak = yes

445.gobmk: -prof-gen(pass 1)  -prof-use(pass 2)  -xCORE-AVX512(pass 2)
 -par-num-threads=1(pass 1)  -ipo(pass 2)  -O3(pass 2)
 -no-prec-div(pass 2)  -qopt-mem-layout-trans=3

456.hmmer: -xCORE-AVX512  -ipo  -O3  -no-prec-div  -unroll2  -auto-ilp32
 -qopt-mem-layout-trans=3

458.sjeng: -prof-gen(pass 1)  -prof-use(pass 2)  -xCORE-AVX512(pass 2)
 -par-num-threads=1(pass 1)  -ipo(pass 2)  -O3(pass 2)
 -no-prec-div(pass 2)  -unroll4  -auto-ilp32
 -qopt-mem-layout-trans=3

462.libquantum: basepeak = yes

464.h264ref: -prof-gen(pass 1)  -prof-use(pass 2)  -xCORE-AVX512(pass 2)
 -par-num-threads=1(pass 1)  -ipo(pass 2)  -O3(pass 2)
 -no-prec-div(pass 2)  -unroll2  -qopt-mem-layout-trans=3

C++ benchmarks:
471.omnetpp: -prof-gen(pass 1)  -prof-use(pass 2)  -xCORE-AVX512(pass 2)
 -par-num-threads=1(pass 1)  -ipo(pass 2)  -O3(pass 2)
 -no-prec-div(pass 2)
 -qopt-ra-region-strategy=block
 -qopt-mem-layout-trans=3  -Wl,-z,muldefs
 -L/sh10.2  -lsmartheap

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Peak Optimization Flags (Continued)

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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