Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6142M, 2.60GHz)

SPECfp®2006 = 152
SPECfp_base2006 = 146

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

CPU Name: Intel Xeon Gold 6142M
CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
CPU MHz: 2600
FPU: Integrated
CPU(s) enabled: 64 cores, 4 chips, 16 cores/chip
CPU(s) orderable: 2,4 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core

Hardware

Software

Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)

Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6142M, 2.60GHz)

SPEC CFP2006 Result
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SPECfp2006 = 152
SPECfp_base2006 = 146

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
L3 Cache: 22 MB I+D on chip per chip
Other Cache: None
Memory: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 1 TB SAS HDD, 7.2K RPM
Other Hardware: None
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other Software: None

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>6.24</td>
<td>2180</td>
<td>6.26</td>
<td>2170</td>
<td>6.28</td>
<td>2170</td>
<td>6.24</td>
<td>2180</td>
<td>6.26</td>
<td>2170</td>
<td>6.28</td>
<td>2170</td>
</tr>
<tr>
<td>416.gamess</td>
<td>404</td>
<td>48.5</td>
<td>404</td>
<td>48.4</td>
<td>404</td>
<td>48.5</td>
<td>380</td>
<td>51.5</td>
<td>379</td>
<td>51.7</td>
<td>379</td>
<td>51.7</td>
</tr>
<tr>
<td>433.milc</td>
<td>119</td>
<td>77.2</td>
<td>118</td>
<td>77.8</td>
<td>119</td>
<td>77.4</td>
<td>119</td>
<td>77.2</td>
<td>118</td>
<td>77.8</td>
<td>119</td>
<td>77.4</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>46.1</td>
<td>197</td>
<td>45.7</td>
<td>199</td>
<td>45.1</td>
<td>202</td>
<td>46.1</td>
<td>197</td>
<td>45.7</td>
<td>199</td>
<td>45.1</td>
<td>202</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>135</td>
<td>53.0</td>
<td>135</td>
<td>52.9</td>
<td>135</td>
<td>53.0</td>
<td>135</td>
<td>53.0</td>
<td>135</td>
<td>52.9</td>
<td>135</td>
<td>53.0</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>8.58</td>
<td>1390</td>
<td>8.61</td>
<td>1390</td>
<td>8.71</td>
<td>1370</td>
<td>8.58</td>
<td>1390</td>
<td>8.61</td>
<td>1390</td>
<td>8.71</td>
<td>1370</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>26.1</td>
<td>360</td>
<td>25.7</td>
<td>365</td>
<td>25.7</td>
<td>365</td>
<td>26.1</td>
<td>360</td>
<td>25.7</td>
<td>365</td>
<td>25.7</td>
<td>365</td>
</tr>
<tr>
<td>444.namd</td>
<td>225</td>
<td>35.7</td>
<td>225</td>
<td>35.7</td>
<td>225</td>
<td>35.7</td>
<td>220</td>
<td>36.5</td>
<td>219</td>
<td>36.6</td>
<td>219</td>
<td>36.6</td>
</tr>
<tr>
<td>447.dealII</td>
<td>158</td>
<td>72.2</td>
<td>158</td>
<td>72.3</td>
<td>158</td>
<td>72.3</td>
<td>158</td>
<td>72.2</td>
<td>158</td>
<td>72.3</td>
<td>158</td>
<td>72.3</td>
</tr>
<tr>
<td>450.soplex</td>
<td>164</td>
<td>50.8</td>
<td>164</td>
<td>50.9</td>
<td>163</td>
<td>51.3</td>
<td>164</td>
<td>50.8</td>
<td>164</td>
<td>50.9</td>
<td>163</td>
<td>51.3</td>
</tr>
<tr>
<td>453.povray</td>
<td>76.3</td>
<td>69.7</td>
<td>76.5</td>
<td>69.6</td>
<td>76.2</td>
<td>69.8</td>
<td>67.3</td>
<td>79.0</td>
<td>67.2</td>
<td>79.2</td>
<td>67.3</td>
<td>79.0</td>
</tr>
<tr>
<td>454.calculix</td>
<td>112</td>
<td>73.4</td>
<td>113</td>
<td>73.3</td>
<td>113</td>
<td>73.3</td>
<td>107</td>
<td>77.0</td>
<td>107</td>
<td>76.9</td>
<td>107</td>
<td>77.0</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>63.3</td>
<td>168</td>
<td>63.0</td>
<td>169</td>
<td>65.5</td>
<td>162</td>
<td>59.1</td>
<td>180</td>
<td>58.9</td>
<td>180</td>
<td>56.5</td>
<td>188</td>
</tr>
<tr>
<td>465.tonto</td>
<td>191</td>
<td>51.6</td>
<td>204</td>
<td>48.2</td>
<td>207</td>
<td>47.5</td>
<td>149</td>
<td>66.3</td>
<td>148</td>
<td>66.5</td>
<td>148</td>
<td>66.5</td>
</tr>
<tr>
<td>470.lbm</td>
<td>5.06</td>
<td>2720</td>
<td>5.25</td>
<td>2620</td>
<td>5.13</td>
<td>2680</td>
<td>5.06</td>
<td>2720</td>
<td>5.25</td>
<td>2620</td>
<td>5.13</td>
<td>2680</td>
</tr>
<tr>
<td>481.wrf</td>
<td>83.7</td>
<td>133</td>
<td>84.0</td>
<td>133</td>
<td>83.8</td>
<td>133</td>
<td>83.7</td>
<td>133</td>
<td>84.0</td>
<td>133</td>
<td>83.8</td>
<td>133</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>261</td>
<td>74.6</td>
<td>260</td>
<td>74.9</td>
<td>261</td>
<td>74.5</td>
<td>261</td>
<td>74.6</td>
<td>260</td>
<td>74.9</td>
<td>261</td>
<td>74.5</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-p0v5 Sat Sep 9 11:10:03 2017
Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6142M, 2.60GHz)

SPECfp2006 = 152
SPECfp_base2006 = 146

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
  4 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
cache size : 22528 KB

From /proc/meminfo
MemTotal: 791967264 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"
    ANSI_COLOR="0;32"
    CPE_NAME=cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-p0v5 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
  (9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Sep 9 11:08

SPEC is set to: /home/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 930G 11G 920G 2% /
Additional information from dmidecode:
Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6142M, 2.60GHz)

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<th>152</th>
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
  icc -m64

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Benchmarks using both Fortran and C:
  icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main

Continued on next page
**Cisco Systems**
Cisco UCS C480 M5 (Intel Xeon Gold 6142M, 2.60GHz)

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**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Test date:** Sep-2017  
**Tested by:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Software Availability:** Apr-2017  

### Base Portability Flags (Continued)

- 437.leslie3d: -DSPEC_CPU_LP64
- 444.namd: -DSPEC_CPU_LP64
- 447.dealII: -DSPEC_CPU_LP64
- 450.soplex: -DSPEC_CPU_LP64
- 453.povray: -DSPEC_CPU_LP64
- 454.calculix: -DSPEC_CPU_LP64 -nofor_main
- 459.GemsFDTD: -DSPEC_CPU_LP64
- 465.tonto: -DSPEC_CPU_LP64
- 470.lbm: -DSPEC_CPU_LP64
- 481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
- 482.sphinx3: -DSPEC_CPU_LP64

### Base Optimization Flags

**C benchmarks:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

**C++ benchmarks:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

**Fortran benchmarks:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

**Benchmarks using both Fortran and C:**
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

### Peak Compiler Invocation

**C benchmarks:**
icc -m64

**C++ benchmarks:**
icpc -m64

**Fortran benchmarks:**
ifort -m64

**Benchmarks using both Fortran and C:**
icc -m64 ifort -m64

### Peak Portability Flags

Same as Base Portability Flags
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6142M, 2.60GHz)

SPECfp2006 = 152
SPECfp_base2006 = 146

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags

C benchmarks:
433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:
444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -fno-alias -auto-ll32
447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-
434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes
459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -unroll2 -inline-level=0 -qopt-prefetch -parallel
465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -inline-call -qopt-malloc-options=3
    -auto -unroll4

Benchmarks using both Fortran and C:
435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes
## Cisco Systems

**Cisco UCS C480 M5 (Intel Xeon Gold 6142M, 2.60GHz)**

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<th>152</th>
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</table>

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**Software Availability:** Apr-2017

<table>
<thead>
<tr>
<th>Peak Optimization Flags (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>454.calculix: -xCORE-AVX2 -ipo -03 -no-prec-div -auto-ilp32</td>
</tr>
<tr>
<td>481.wrf: basepeak = yes</td>
</tr>
</tbody>
</table>

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html  
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml  
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For other inquiries, please contact webmaster@spec.org.

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