Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

<table>
<thead>
<tr>
<th>SPECint®2006 = 79.4</th>
<th>SPECint_base2006 = 75.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2006 license: 9019</td>
<td>Test date: Sep-2017</td>
</tr>
<tr>
<td>Test sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Apr-2017</td>
</tr>
</tbody>
</table>

### Hardware

<table>
<thead>
<tr>
<th>Component</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Gold 6142M</td>
</tr>
<tr>
<td>CPU Characteristics</td>
<td>Intel Turbo Boost Technology up to 3.70 GHz</td>
</tr>
<tr>
<td>CPU MHZ</td>
<td>2600</td>
</tr>
<tr>
<td>FPU</td>
<td>Integrated</td>
</tr>
<tr>
<td>CPU(s) enabled</td>
<td>32 cores, 2 chips, 16 cores/chip</td>
</tr>
<tr>
<td>CPU(s) orderable</td>
<td>1.2 chips</td>
</tr>
<tr>
<td>Primary Cache</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Secondary Cache</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3 Cache</td>
<td>22 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other Cache</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Disk Subsystem</td>
<td>1 x 600 GB SAS HDD, 10K RPM</td>
</tr>
<tr>
<td>Other Hardware</td>
<td>None</td>
</tr>
</tbody>
</table>

### Software

<table>
<thead>
<tr>
<th>Component</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System</td>
<td>Red Hat Enterprise Linux Server release 7.3 (Maipo) 3.10.0-514.el7.x86_64</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux</td>
</tr>
<tr>
<td>Auto Parallel</td>
<td>Yes</td>
</tr>
<tr>
<td>File System</td>
<td>xfs</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other Software</td>
<td>Microquill SmartHeap V10.2</td>
</tr>
</tbody>
</table>
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbch</td>
<td>209</td>
<td>46.6</td>
<td>209</td>
<td>46.7</td>
<td>210</td>
<td>46.5</td>
<td>185</td>
<td>52.9</td>
<td>185</td>
<td>52.8</td>
<td>184</td>
<td>53.1</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>341</td>
<td>28.3</td>
<td>340</td>
<td>28.3</td>
<td>341</td>
<td>28.3</td>
<td>338</td>
<td>28.6</td>
<td>338</td>
<td>28.5</td>
<td>338</td>
<td>28.5</td>
</tr>
<tr>
<td>403.mcf</td>
<td>186</td>
<td>43.2</td>
<td>186</td>
<td>43.3</td>
<td>186</td>
<td>43.2</td>
<td>182</td>
<td>44.3</td>
<td>182</td>
<td>44.3</td>
<td>182</td>
<td>44.3</td>
</tr>
<tr>
<td>429.gcc</td>
<td>114</td>
<td>79.9</td>
<td>116</td>
<td>78.5</td>
<td>115</td>
<td>79.1</td>
<td>115</td>
<td>79.4</td>
<td>117</td>
<td>77.7</td>
<td>115</td>
<td>79.2</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>312</td>
<td>33.6</td>
<td>313</td>
<td>33.6</td>
<td>313</td>
<td>33.5</td>
<td>310</td>
<td>33.8</td>
<td>311</td>
<td>33.8</td>
<td>310</td>
<td>33.8</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>96.6</td>
<td>96.6</td>
<td>96.6</td>
<td>96.6</td>
<td>96.5</td>
<td>96.7</td>
<td>96.6</td>
<td>96.6</td>
<td>96.6</td>
<td>96.6</td>
<td>96.5</td>
<td>96.7</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>326</td>
<td>37.1</td>
<td>326</td>
<td>37.1</td>
<td>326</td>
<td>37.1</td>
<td>320</td>
<td>37.8</td>
<td>320</td>
<td>37.8</td>
<td>320</td>
<td>37.8</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>2.50</td>
<td>8280</td>
<td>2.52</td>
<td>8230</td>
<td>2.51</td>
<td>8270</td>
<td>2.50</td>
<td>8280</td>
<td>2.52</td>
<td>8230</td>
<td>2.51</td>
<td>8270</td>
</tr>
<tr>
<td>464.h264ref</td>
<td>317</td>
<td>69.9</td>
<td>317</td>
<td>69.9</td>
<td>316</td>
<td>70.0</td>
<td>317</td>
<td>69.9</td>
<td>317</td>
<td>69.9</td>
<td>316</td>
<td>70.0</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>172</td>
<td>36.3</td>
<td>172</td>
<td>36.4</td>
<td>172</td>
<td>36.3</td>
<td>130</td>
<td>48.3</td>
<td>129</td>
<td>48.4</td>
<td>130</td>
<td>48.0</td>
</tr>
<tr>
<td>473.astar</td>
<td>181</td>
<td>38.8</td>
<td>181</td>
<td>38.7</td>
<td>181</td>
<td>38.7</td>
<td>181</td>
<td>38.7</td>
<td>182</td>
<td>38.7</td>
<td>182</td>
<td>38.7</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>86.7</td>
<td>79.6</td>
<td>86.7</td>
<td>79.6</td>
<td>86.7</td>
<td>79.6</td>
<td>78.3</td>
<td>88.1</td>
<td>77.7</td>
<td>88.8</td>
<td>77.7</td>
<td>88.8</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The config file option 'submit' was used.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Platform Notes

- BIOS Settings:
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS
  - SNC set to Disabled
  - IMC Interleaving set to Auto
  - Patrol Scrub set to Disabled

- Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
  - Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
  - running on localhost.localdomain Sun Sep 10 14:36:31 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:

- [http://www.spec.org/cpu2006/Docs/config.html#sysinfo](http://www.spec.org/cpu2006/Docs/config.html#sysinfo)

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Gold 6142M CPU @ 2.60GHz
- 2 "physical id"s (chips)
- 32 "processors"

Continued on next page
Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECint2006 = 79.4
SPECint_base2006 = 75.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)

```
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
cache size : 22528 KB
```

From /proc/meminfo
```
MemTotal: 394867072 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
```

From /etc/*release* /etc/*version*
```
os-release:
NAME="Red Hat Enterprise Linux Server"
VERSION="7.3 (Maipo)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="7.3"
PRETTY_NAME="Red Hat Enterprise Linux Server 7.3 (Maipo)"
ANSI_COLOR="0;31"
CPE_NAME="cpe:/o:redhat:enterprise_linux:7.3:GA:server"
redhat-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)
system-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)
```

uname -a:
```
Linux localhost.localdomain 3.10.0-514.el7.x86_64 #1 SMP Wed Oct 19 11:24:13 EDT 2016 x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Sep 10 01:38

SPEC is set to: /home/cpu2006-1.2
```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda2 xfs 501G 13G 488G 3% /
```

Additional information from dmidecode:
```
Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017Cisco Systems, Inc. C240M5.3.1.1d.0.0615170707 06/15/2017
Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz
```

(End of data from sysinfo program)
The correct amount of Memory installed is 384 GB (24 x 16 GB)
and the dmidecode is reporting invalid number of DIMMs installed

Continued on next page
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECint2006 = 79.4
SPECint_base2006 = 75.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

Installed Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "32"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch
-auto-p32
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECint2006 = 79.4
SPECint_base2006 = 75.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Base Optimization Flags (Continued)

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
-W1,-z,muldefs -L/sh10.2 -lsmartheap64

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64
400.perlbench: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
445.gobmk: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

C++ benchmarks (except as noted below):
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

SPECint2006 = 79.4
SPECint_base2006 = 75.7

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags

C benchmarks:
400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div(pass 2) -qopt-prefetch
401.bzip2:  -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
               -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
               -no-prec-div -auto-ilp32 -qopt-prefetch
403.gcc:  -xCORE-AVX2 -ipo -O3 -no-prec-div -inline-calloc
          -qopt-malloc-options=3 -auto-ilp32
429.mcf:  -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
          -qopt-prefetch -auto-p32
445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
            -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
            -no-prec-div(pass 2)
456.hmmer: basepeak = yes
458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
            -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
            -no-prec-div(pass 2) -unroll4
462.libquantum: basepeak = yes
464.h264ref: basepeak = yes

C++ benchmarks:
471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
             -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
             -no-prec-div(pass 2) -qopt-ra-region-strategy=block
             -Wl,-z,muldefs -L/sh10.2 -lsmartheap
473.astar:  -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
             -auto-p32 -Wl,-z,muldefs -L/sh10.2 -lsmartheap64
483.xalancbmk: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
               -Wl,-z,muldefs -L/sh10.2 -lsmartheap

Peak Other Flags

C benchmarks:

Continued on next page
## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6142M 2.60 GHz)

| SPECint2006 = | 79.4 |
| SPECint_base2006 = | 75.7 |

### CPU2006 Details

| CPU2006 license: | 9019 |
| Test sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |

### Test Details

| Test date: | Sep-2017 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Apr-2017 |

### Peak Other Flags (Continued)

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at

- [Intel-ic17.0-official-linux64-revF.html](http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html)
- [Cisco-Platform-Settings-V1.2-revH.html](http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html)

You can also download the XML flags sources by saving the following links:

- [Intel-ic17.0-official-linux64-revF.xml](http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml)
- [Cisco-Platform-Settings-V1.2-revH.xml](http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml)

---

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.

For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.


Originally published on 12 October 2017.