Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPECfp®2006 = 131
SPECfp_base2006 = 125

Hardware
CPU Name: Intel Xeon Gold 5120
CPU Characteristics: Intel Turbo Boost Technology up to 3.20 GHz
CPU MHz: 2200
FPU: Integrated
CPU(s) enabled: 28 cores, 2 chips, 14 cores/chip
CPU(s) orderable: 1.2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core

Software
Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
Cisco Systems

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SPEC CFP2006 Result

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L3 Cache: 19.25 MB I+D on chip per chip
Other Cache: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400 MHz)
Disk Subsystem: 1 x 1 TB SAS HDD, 7.2K RPM
Other Hardware: None

Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other Software: None

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>15.8</td>
<td>862</td>
<td>15.5</td>
<td>877</td>
<td>15.5</td>
<td>877</td>
<td>15.8</td>
<td>862</td>
<td>15.5</td>
<td>877</td>
</tr>
<tr>
<td>416.gamess</td>
<td>482</td>
<td>40.6</td>
<td>483</td>
<td>40.6</td>
<td>482</td>
<td>40.6</td>
<td>439</td>
<td>44.6</td>
<td>438</td>
<td>44.7</td>
</tr>
<tr>
<td>433.milc</td>
<td>126</td>
<td>72.6</td>
<td>129</td>
<td>71.4</td>
<td>127</td>
<td>72.2</td>
<td>126</td>
<td>72.6</td>
<td>129</td>
<td>71.4</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>38.5</td>
<td>236</td>
<td>38.4</td>
<td>237</td>
<td>38.4</td>
<td>237</td>
<td>38.5</td>
<td>236</td>
<td>38.4</td>
<td>237</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>162</td>
<td>44.2</td>
<td>162</td>
<td>44.0</td>
<td>162</td>
<td>44.1</td>
<td>162</td>
<td>44.2</td>
<td>162</td>
<td>44.0</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>10.1</td>
<td>1190</td>
<td>10.2</td>
<td>1180</td>
<td>10.0</td>
<td>1190</td>
<td>10.1</td>
<td>1190</td>
<td>10.2</td>
<td>1180</td>
</tr>
<tr>
<td>444.namd</td>
<td>263</td>
<td>30.5</td>
<td>261</td>
<td>30.7</td>
<td>262</td>
<td>30.6</td>
<td>255</td>
<td>31.5</td>
<td>254</td>
<td>31.6</td>
</tr>
<tr>
<td>447.dealII</td>
<td>179</td>
<td>63.8</td>
<td>181</td>
<td>63.3</td>
<td>180</td>
<td>63.5</td>
<td>179</td>
<td>63.8</td>
<td>181</td>
<td>63.3</td>
</tr>
<tr>
<td>450.soplex</td>
<td>188</td>
<td>44.3</td>
<td>188</td>
<td>44.3</td>
<td>189</td>
<td>44.2</td>
<td>188</td>
<td>44.3</td>
<td>188</td>
<td>44.3</td>
</tr>
<tr>
<td>453.povray</td>
<td>88.4</td>
<td>60.2</td>
<td>88.8</td>
<td>59.9</td>
<td>88.7</td>
<td>60.0</td>
<td>78.1</td>
<td>68.1</td>
<td>78.3</td>
<td>68.0</td>
</tr>
<tr>
<td>454.calculix</td>
<td>130</td>
<td>63.5</td>
<td>131</td>
<td>63.2</td>
<td>130</td>
<td>63.3</td>
<td>124</td>
<td>66.4</td>
<td>125</td>
<td>66.1</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>39.2</td>
<td>270</td>
<td>38.4</td>
<td>276</td>
<td>37.8</td>
<td>280</td>
<td>31.9</td>
<td>33.3</td>
<td>32.0</td>
<td>332</td>
</tr>
<tr>
<td>465.tonto</td>
<td>238</td>
<td>41.4</td>
<td>240</td>
<td>41.1</td>
<td>237</td>
<td>41.6</td>
<td>169</td>
<td>58.3</td>
<td>168</td>
<td>58.4</td>
</tr>
<tr>
<td>470.lbm</td>
<td>11.0</td>
<td>1240</td>
<td>11.0</td>
<td>1250</td>
<td>11.0</td>
<td>1250</td>
<td>11.0</td>
<td>1240</td>
<td>11.0</td>
<td>1250</td>
</tr>
<tr>
<td>481.wrf</td>
<td>97.7</td>
<td>114</td>
<td>97.3</td>
<td>115</td>
<td>98.5</td>
<td>113</td>
<td>97.7</td>
<td>114</td>
<td>97.3</td>
<td>115</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>332</td>
<td>58.7</td>
<td>327</td>
<td>59.6</td>
<td>326</td>
<td>59.7</td>
<td>332</td>
<td>58.7</td>
<td>327</td>
<td>59.6</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
Continued on next page
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SPECfp2006 = 131
SPECfp_base2006 = 125

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

running on linux-uezu Wed Sep 27 07:05:30 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5120 CPU @ 2.20GHz
  2 "physical id"s (chips)
  28 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 14
  siblings : 14
  physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
  physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14
  cache size : 19712 KB

From /proc/meminfo
MemTotal: 394832632 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or release.
  # Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME=cpe:/o:suse:sles:12:sp2"

uname -a:
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 6 13:34

SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdal xfs 894G 57G 838G 7% /

Additional information from dmidecode:

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SPEC CFP2006 Result

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| SPECfp2006 | 131 |
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CPU2006 license: 9019
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Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory: 24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz, configured at 2400 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/opt/intel/compilers_and_libraries_2018.0.128/linux/compiler/lib/ia32:/opt/intel/compilers_and_libraries_2018.0.128/linux/compiler/lib/intel64:/opt/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "28"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64

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### Base Portability Flags (Continued)

- 444.namd: -DSPEC_CPU_LP64
- 447.dealII: -DSPEC_CPU_LP64
- 450.soplex: -DSPEC_CPU_LP64
- 453.povray: -DSPEC_CPU_LP64
- 454.calculix: -DSPEC_CPU_LP64 -nofor_main
- 459.GemsFDTD: -DSPEC_CPU_LP64
- 465.tonto: -DSPEC_CPU_LP64
- 470.lbm: -DSPEC_CPU_LP64
- 481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
- 482.sphinx3: -DSPEC_CPU_LP64

### Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

### Peak Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

### Peak Portability Flags

Same as Base Portability Flags
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CPU2006 license: 9019
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Tested by: Cisco Systems

Test date: Sep-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags

C benchmarks:

433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:

444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -fno-alias -auto-ilp32

447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:

410.bwaves: basepeak = yes
416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-

434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes

459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -qopt-prefetch -parallel

465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -inline-calloc -qopt-malloc-options=3
-auto -unroll4

Benchmarks using both Fortran and C:

435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes

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Cisco UCS B200 M5 (Intel Xeon Gold 5120, 2.20GHz)

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<th>SPECfp2006</th>
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<th>Hardware Availability</th>
<th>Tested by</th>
<th>Software Availability</th>
</tr>
</thead>
</table>

### Peak Optimization Flags (Continued)

454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-ilp32

481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For other inquiries, please contact webmaster@spec.org.

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