Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

SPECfp®2006 = 161
SPECfp_base2006 = 156

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Hardware
CPU Name: Intel Xeon Gold 6146
CPU Characteristics: Intel Turbo Boost Technology up to 4.20 GHz
CPU MHz: 3200
FPU: Integrated
CPU(s) enabled: 48 cores, 4 chips, 12 cores/chip
CPU(s) orderable: 2, 4 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core

Software
Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)

Copyright 2006-2017 Standard Performance Evaluation Corporation

Continued on next page
## SPEC CFP2006 Result

### Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Base</th>
<th>Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Seconds</td>
<td>Ratio</td>
</tr>
<tr>
<td>410.bwaves</td>
<td>8.57</td>
<td>1590</td>
</tr>
<tr>
<td>416.gamess</td>
<td>371</td>
<td>52.8</td>
</tr>
<tr>
<td>433.milc</td>
<td><strong>114</strong></td>
<td><strong>80.6</strong></td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>39.9</td>
<td>228</td>
</tr>
<tr>
<td>435.gromacs</td>
<td><strong>115</strong></td>
<td><strong>62.0</strong></td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>8.37</td>
<td>1430</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>22.5</td>
<td>417</td>
</tr>
<tr>
<td>444.namd</td>
<td>198</td>
<td>40.5</td>
</tr>
<tr>
<td>447.dealII</td>
<td>143</td>
<td>80.1</td>
</tr>
<tr>
<td>450.soplex</td>
<td>146</td>
<td>57.2</td>
</tr>
<tr>
<td>453.povray</td>
<td><strong>67.3</strong></td>
<td><strong>79.1</strong></td>
</tr>
<tr>
<td>454.calculix</td>
<td><strong>105</strong></td>
<td><strong>78.4</strong></td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>57.7</td>
<td>184</td>
</tr>
<tr>
<td>465.tonto</td>
<td><strong>181</strong></td>
<td><strong>54.3</strong></td>
</tr>
<tr>
<td>470.lbm</td>
<td>5.27</td>
<td>2610</td>
</tr>
<tr>
<td>481.wrf</td>
<td>81.3</td>
<td>137</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td><strong>240</strong></td>
<td><strong>81.3</strong></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise
- Power Performance Tuning set to OS
- SNC set to Disabled
- IMC Interleaving set to Auto
- Patrol Scrub set to Disabled

Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-vb5q Mon Jan 4 23:06:41 2010
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

SPECfp2006 = 161
SPECfp_base2006 = 156

CPU2006 license: 9019
Test date: Nov-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
4 "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
physical 0: cores 0 3 4 5 6 7 16 18 19 20 21 22
physical 1: cores 0 3 4 5 6 7 16 18 19 20 21 22
physical 2: cores 0 1 3 9 10 16 18 19 24 25 26 27
physical 3: cores 0 1 3 9 10 16 18 19 24 25 26 27
cache size : 25344 KB

From /proc/meminfo
MemTotal:       791029124 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-vb5q 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
(9464f67) x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Jan 4 23:04

SPEC is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 280G 105G 176G 38% /
Additional information from dmidecode:
Continued on next page
Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

SPECfp2006 = 161
SPECfp_base2006 = 156

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017
Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib/ia32:/opt/cpu2006-1.2/lib/intel64:/opt/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "48"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main

Continued on next page
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

SPECfp2006 = 161
SPECfp_base2006 = 156

CPU2006 license: 9019
Test date: Nov-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Apr-2017

Base Portability Flags (Continued)

437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Peak Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Peak Portability Flags

Same as Base Portability Flags
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

SPEC CFP2006 Result

SPECfp2006 = 161
SPECfp_base2006 = 156

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags

C benchmarks:
433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:
444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -fno-alias -auto-ilp32

447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-

434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes
459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -qopt-prefetch -parallel

465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -inline-calloc -qopt-malloc-options=3
-auto -unroll4

Benchmarks using both Fortran and C:
435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes

Continued on next page
## Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

<table>
<thead>
<tr>
<th>SPECfp2006</th>
<th>161</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECfp_base2006</td>
<td>156</td>
</tr>
</tbody>
</table>

| CPU2006 license: | 9019 |
| Test sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test date: | Nov-2017 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Apr-2017 |

### Peak Optimization Flags (Continued)

- 454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-llp32
- 481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:


---

SPEC and SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.

For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.


Originally published on 26 December 2017.