Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPEClnt®2006 = 79.1
SPEClnt_base2006 = 75.4

Hardware
CPU Name: Intel Xeon Gold 6130
CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz
CPU MHz: 2100
FPU: Integrated
CPU(s) enabled: 32 cores, 2 chips, 16 cores/chip
CPU(s) orderable: 1.2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core
L3 Cache: None
Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem: 1 x 600 GB SAS HDD, 10K RPM
Other Hardware: None

Software
Operating System: Red Hat Enterprise Linux Server release 7.3 (Maipo) 3.10.0-514.el7.x86_64
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 32/64-bit
Peak Pointers: 32/64-bit
Other Software: Microquill SmartHeap V10.2
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint2006 = 79.1
SPECint_base2006 = 75.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>209</td>
<td>46.7</td>
<td>209</td>
<td>46.7</td>
<td>209</td>
<td>46.6</td>
<td>184</td>
<td>53.2</td>
<td>184</td>
<td>53.2</td>
</tr>
<tr>
<td>403.gcc</td>
<td>181</td>
<td>44.5</td>
<td>181</td>
<td>44.5</td>
<td>181</td>
<td>44.4</td>
<td>178</td>
<td>45.3</td>
<td>178</td>
<td>45.3</td>
</tr>
<tr>
<td>429.mcf</td>
<td>114</td>
<td>79.8</td>
<td>114</td>
<td>79.7</td>
<td>113</td>
<td>80.5</td>
<td>113</td>
<td>80.4</td>
<td>114</td>
<td>79.8</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>312</td>
<td>33.6</td>
<td>312</td>
<td>33.6</td>
<td>312</td>
<td>33.6</td>
<td>309</td>
<td>33.9</td>
<td>309</td>
<td>33.9</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>96.1</td>
<td>97.1</td>
<td>96.1</td>
<td>97.1</td>
<td>96.3</td>
<td>96.9</td>
<td>96.1</td>
<td>97.1</td>
<td>96.1</td>
<td>96.9</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>324</td>
<td>37.3</td>
<td>324</td>
<td>37.3</td>
<td>324</td>
<td>37.3</td>
<td>317</td>
<td>38.1</td>
<td>317</td>
<td>38.1</td>
</tr>
<tr>
<td>462.libquantum</td>
<td>2.83</td>
<td>7330</td>
<td>2.79</td>
<td>7410</td>
<td>2.81</td>
<td>7380</td>
<td>2.83</td>
<td>7330</td>
<td>2.79</td>
<td>7410</td>
</tr>
<tr>
<td>464.hmmer</td>
<td>328</td>
<td>67.4</td>
<td>327</td>
<td>67.6</td>
<td>328</td>
<td>67.5</td>
<td>328</td>
<td>67.4</td>
<td>327</td>
<td>67.6</td>
</tr>
<tr>
<td>471.omnetpp</td>
<td>173</td>
<td>36.2</td>
<td>172</td>
<td>36.3</td>
<td>172</td>
<td>36.2</td>
<td>128</td>
<td>48.9</td>
<td>129</td>
<td>48.5</td>
</tr>
<tr>
<td>473.astar</td>
<td>179</td>
<td>39.2</td>
<td>180</td>
<td>39.1</td>
<td>180</td>
<td>38.9</td>
<td>179</td>
<td>39.3</td>
<td>179</td>
<td>39.2</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>82.6</td>
<td>83.5</td>
<td>82.6</td>
<td>83.5</td>
<td>82.6</td>
<td>83.6</td>
<td>75.6</td>
<td>91.2</td>
<td>76.6</td>
<td>90.0</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The config file option 'submit' was used.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on localhost.localdomain Thu Nov 16 01:01:43 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6130 CPU @ 2.10GHz
 2 "physical id"s (chips)
 32 "processors"

Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint2006 = 79.1
SPECint_base2006 = 75.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
cpu cores : 16
siblings : 16
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
cache size : 22528 KB

From /proc/meminfo
MemTotal: 394670188 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="Red Hat Enterprise Linux Server"
VERSION="7.3 (Maipo)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="7.3"
PRETTY_NAME="Red Hat Enterprise Linux Server 7.3 (Maipo)"
ANSI_COLOR="0;31"
CPE_NAME="cpe:/o:redhat:enterprise_linux:7.3:GA:server"
redhat-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)
system-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)

uname -a:
Linux localhost.localdomain 3.10.0-514.el7.x86_64 #1 SMP Wed Oct 19 11:24:13
EDT 2016 x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 8 20:26
SPECl is set to: /opt/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb2 xfs 130G 14G 117G 11% /

Additional information from dmidecode:
Warning: Use caution when you interpret this section. The 'dmidecode' program
reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017Cisco Systems,
Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
48x 0xCE00 M393A2G40BB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)
The correct amount of Memory installed is 384 GB (24 x 16 GB)
and the dmidecode is reporting invalid number of DIMMs installed
Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint2006 = 79.1
SPECint_base2006 = 75.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Platform Notes (Continued)

Installed Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/lib/ia32:/opt/cpu2006-1.2/lib/intel64:/opt/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "32"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Base Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -DSPEC_CPU_LP64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -DSPEC_CPU_LP64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -03 -no-prec-div -parallel -qopt-prefetch
-auto-p32

Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint2006 = 79.1
SPECint_base2006 = 75.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Nov-2017
 Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Base Optimization Flags (Continued)

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
-Wl,-z,muldefs -L/sh10.2 -lsmartheap64

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64
400.perlbench: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
445.gobmk: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32

C++ benchmarks (except as noted below):
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
473.astar: icpc -m64

Peak Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint2006 = 79.1
SPECint_base2006 = 75.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Nov-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-prefetch

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div -auto-ilp32 -qopt-prefetch

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div -inline-calloc
-qopt-malloc-options=3 -auto-ilp32

429.mcf: -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
-qopt-prefetch -auto-p32

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2)

456.hmmer: basepeak = yes

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4

462.libquantum: basepeak = yes

464.h264ref: basepeak = yes

C++ benchmarks:

471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-ra-region-strategy=block
-Wl,-z,muldefs -L/sh10.2 -lsmartheap

473.astar: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-auto-p32 -Wl,-z,muldefs -L/sh10.2 -lsmartheap64

483.xalancbmk: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-Wl,-z,muldefs -L/sh10.2 -lsmartheap

Peak Other Flags

C benchmarks:

Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6130, 2.10 GHz)

SPECint2006 = 79.1
SPECint_base2006 = 75.4

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017

Peak Other Flags (Continued)

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC and SPECint are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.
Originally published on 26 December 2017.