Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Silver 4108, 1.80 GHz)

<table>
<thead>
<tr>
<th>SPECfp®2006</th>
<th>SPECfp_base2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>109</td>
<td>103</td>
</tr>
</tbody>
</table>

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Software</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Silver 4108</td>
<td>Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default</td>
</tr>
<tr>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 3.00 GHz</td>
<td>Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux; Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>CPU MHz: 1800</td>
<td>Auto Parallel: Yes</td>
</tr>
<tr>
<td>FPU: Integrated</td>
<td>File System: xfs</td>
</tr>
<tr>
<td>CPU(s) enabled: 16 cores, 2 chips, 8 cores/chip</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>CPU(s) orderable: 1,2 chips</td>
<td></td>
</tr>
<tr>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
<td></td>
</tr>
<tr>
<td>Secondary Cache: 1 MB I+D on chip per core</td>
<td></td>
</tr>
</tbody>
</table>

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jun-2017
# SPEC CFP2006 Result

## Cisco Systems

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<tr>
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</tr>
</tbody>
</table>

- **L3 Cache:** 11 MB I+D on chip per chip
- **Other Cache:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Disk Subsystem:** 1 x 600 GB SAS HDD, 10K RPM
- **Other Hardware:** None
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other Software:** None

### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>19.3</td>
<td>704</td>
<td>19.1</td>
<td>712</td>
<td><strong>19.2</strong></td>
<td><strong>710</strong></td>
<td>19.3</td>
<td>704</td>
</tr>
<tr>
<td>416.gamess</td>
<td>543</td>
<td>36.1</td>
<td>543</td>
<td>36.1</td>
<td><strong>543</strong></td>
<td><strong>36.1</strong></td>
<td>470</td>
<td>41.6</td>
</tr>
<tr>
<td>433.milc</td>
<td><strong>135</strong></td>
<td><strong>68.0</strong></td>
<td>135</td>
<td>68.0</td>
<td>136</td>
<td>67.4</td>
<td>135</td>
<td><strong>68.0</strong></td>
</tr>
<tr>
<td>434.zeusmp</td>
<td><strong>48.4</strong></td>
<td><strong>188</strong></td>
<td>48.3</td>
<td>188</td>
<td>48.5</td>
<td>188</td>
<td><strong>48.4</strong></td>
<td><strong>188</strong></td>
</tr>
<tr>
<td>435.gromacs</td>
<td><strong>193</strong></td>
<td><strong>37.1</strong></td>
<td>193</td>
<td>37.1</td>
<td>193</td>
<td>37.0</td>
<td><strong>193</strong></td>
<td><strong>37.1</strong></td>
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<tr>
<td>436.cactusADM</td>
<td><strong>16.1</strong></td>
<td><strong>740</strong></td>
<td>16.1</td>
<td>741</td>
<td>16.2</td>
<td>737</td>
<td><strong>16.1</strong></td>
<td><strong>740</strong></td>
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<tr>
<td>437.leslie3d</td>
<td>28.4</td>
<td>331</td>
<td><strong>28.5</strong></td>
<td><strong>330</strong></td>
<td>28.5</td>
<td>329</td>
<td>28.4</td>
<td>331</td>
</tr>
<tr>
<td>444.namd</td>
<td><strong>278</strong></td>
<td><strong>28.9</strong></td>
<td>278</td>
<td>28.9</td>
<td>278</td>
<td>28.9</td>
<td>271</td>
<td>29.6</td>
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<tr>
<td>447.dealII</td>
<td>193</td>
<td>59.2</td>
<td>192</td>
<td>59.5</td>
<td><strong>192</strong></td>
<td><strong>59.4</strong></td>
<td>193</td>
<td>59.2</td>
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<tr>
<td>450.soplex</td>
<td><strong>213</strong></td>
<td><strong>39.2</strong></td>
<td>214</td>
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<td>212</td>
<td>39.4</td>
<td><strong>213</strong></td>
<td><strong>39.2</strong></td>
</tr>
<tr>
<td>453.povray</td>
<td><strong>94.2</strong></td>
<td><strong>56.5</strong></td>
<td>94.3</td>
<td>56.4</td>
<td>94.2</td>
<td>56.5</td>
<td>83.0</td>
<td>64.1</td>
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<tr>
<td>454.calculix</td>
<td><strong>142</strong></td>
<td><strong>57.9</strong></td>
<td>142</td>
<td>58.0</td>
<td>143</td>
<td>57.8</td>
<td>133</td>
<td>61.9</td>
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<tr>
<td>459.GemsFDTD</td>
<td>50.9</td>
<td>208</td>
<td><strong>50.8</strong></td>
<td><strong>209</strong></td>
<td>49.7</td>
<td>213</td>
<td>44.2</td>
<td>240</td>
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<tr>
<td>465.tonto</td>
<td>278</td>
<td>35.3</td>
<td>279</td>
<td>35.2</td>
<td><strong>279</strong></td>
<td><strong>35.3</strong></td>
<td>185</td>
<td>53.3</td>
</tr>
<tr>
<td>470.lbm</td>
<td><strong>15.1</strong></td>
<td><strong>912</strong></td>
<td>15.0</td>
<td>916</td>
<td>15.1</td>
<td>909</td>
<td><strong>15.1</strong></td>
<td><strong>912</strong></td>
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<tr>
<td>481.wrf</td>
<td>131</td>
<td>85.5</td>
<td>132</td>
<td>84.6</td>
<td><strong>131</strong></td>
<td><strong>85.4</strong></td>
<td>131</td>
<td>85.5</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>407</td>
<td>47.9</td>
<td>409</td>
<td>47.6</td>
<td><strong>408</strong></td>
<td><strong>47.8</strong></td>
<td>407</td>
<td>47.9</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS Controls
  - SNC set to Disabled
  - Patrol Scrub set to Disabled
- **Sysinfo program** /home/cpu2006-1.2/config/sysinfo.rev6993
- Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
- running on linux-3joc Sat Dec 16 19:21:59 2017

Continued on next page
Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7
cache size : 11264 KB

From /proc/meminfo
MemTotal:       394864824 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-3joc 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
  (9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3  Dec  16  19:20

SPEC is set to: /home/cpu2006-1.2
Filesystem     Type  Size  Used  Avail  Use% Mounted on
/dev/sda3      xfs  516G  116G  401G  23%  /home

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Platform Notes (Continued)

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C220M5.3.1.1d.0.0615170645 06/15/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz, configured at 2400 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "16"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled

No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Base Compiler Invocation

C benchmarks:
icc -m64

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Base Compiler Invocation (Continued)

C++ benchmarks:
icpc -m64
Fortran benchmarks:
ifort -m64
Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.games: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64 -nofor_main
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch
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Peak Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:
444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -fno-alias -auto-ilp32
447.dealII: basepeak = yes
450.soplex: basepeak = yes
453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
410.bwaves: basepeak = yes
416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2) -no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-

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Peak Optimization Flags (Continued)

434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes
459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0
-ipo-prefetch -parallel
465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -inline-calloc -ipo-malloc-options=3
-auto -unroll4

Benchmarks using both Fortran and C:
435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes
454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-ilp32
481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For other inquiries, please contact webmaster@spec.org.

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