Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECfp_rate2006</th>
<th>SPECfp_rate_base2006</th>
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<td>436.cactusADM</td>
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<tr>
<td>482.sphinx3</td>
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</tbody>
</table>

Hardware

- **CPU Name:** Intel Xeon Gold 6134M
- **CPU Characteristics:** Intel Turbo Boost Technology up to 3.70 GHz
- **CPU MHz:** 3200
- **FPU:** Integrated
- **CPU(s) enabled:** 16 cores, 2 chips, 8 cores/chip, 2 threads/core
- **CPU(s) orderable:** 1.2 chips
- **Primary Cache:** 32 KB I + 32 KB D on chip per core
- **Secondary Cache:** 1 MB I+D on chip per core

Software

- **Operating System:** SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler:** C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux; Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
- **Auto Parallel:** Yes
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
## SPEC CFP2006 Result

### Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)  
**SPECfp_rate2006 =** 976  
**SPECfp_rate_base2006 =** 960

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<td>Cisco Systems</td>
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<td>Cisco Systems</td>
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<tr>
<td>L3 Cache:</td>
<td>24.75 MB I+D on chip per chip</td>
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<tr>
<td>Other Cache:</td>
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<td>Memory:</td>
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<tr>
<td>Disk Subsystem:</td>
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### Results Table

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<th>Ratio</th>
<th>Peak Seconds</th>
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<td>878</td>
<td>706</td>
<td>883</td>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise

Continued on next page
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

**SPECfp_rate2006 = 976**

**SPECfp_rate_base2006 = 960**

CPU2006 license: 9019  
Test sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test date: Dec-2017  
Hardware Availability: Aug-2017  
Software Availability: Jul-2017

**Platform Notes (Continued)**

Power Performance Tuning set to OS Controls  
SNC set to Enabled  
IMC Interleaving set to 1-way Interleave  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993  
Revision 6993 of 2015-11-06 (b5e9d4b4eb51ed28d7f98696cbe290c1)  
running on linux Wed Dec 20 18:21:05 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:  
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Gold 6134M CPU @ 3.20GHz  
2 "physical id"s (chips)  
32 "processors"  
core(s), siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 8  
siblings : 16  
physical 0: cores 0 2 3 9 16 19 26 27  
physical 1: cores 0 2 3 9 16 19 26 27  
cache size : 25344 KB

From /proc/meminfo  
MemTotal: 395441684 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*  
SuSE-release:  
SUSE Linux Enterprise Server 12 (x86_64)  
VERSION = 12  
PATCHLEVEL = 2  
# This file is deprecated and will be removed in a future service pack or release.  
# Please check /etc/os-release for details about this release.

os-release:  
NAME="SLES"  
VERSION="12-SP2"  
VERSION_ID="12.2"  
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"  
ID="sles"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:  
Linux linux 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)  
x86_64 x86_64 x86_64 GNU/Linux  
run-level 3 Jan 2 17:25
Platform Notes (Continued)

SPEC is set to: /home/cpu2006-1.2
Filesystem     Type  Size  Used  Avail  Use%  Mounted on
/dev/sdal     xfs  280G  146G  134G  53%  /
Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz
(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
umactl --interleave=all runspec <etc>
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPECfp_rate2006 = 976
SPECfp_rate_base2006 = 960

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jul-2017

Base Compiler Invocation

C benchmarks:
  icc -m64

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Benchmarks using both Fortran and C:
  icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
343.milc: -DSPEC_CPU_LP64
344.zeusmp: -DSPEC_CPU_LP64
345.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
  -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
  -qopt-mem-layout-trans=3

C++ benchmarks:
  -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
  -qopt-mem-layout-trans=3

Fortran benchmarks:
  -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPECfp_rate2006 = 976
SPECfp_rate_base2006 = 960

CPU2006 license: 9019
Test sponsor: Cisco Systems
Test date: Dec-2017
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Jul-2017

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32
-qopt-mem-layout-trans=3

Peak Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks (except as noted below):
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Peak Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -D_FILE_OFFSET_BITS=64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Peak Optimization Flags

C benchmarks:

Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPEC CFP2006 Result

**SPECfp_rate2006** = 976  
**SPECfp_rate_base2006** = 960

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<td>Cisco Systems</td>
<td>Software Availability</td>
<td>Jul-2017</td>
</tr>
</tbody>
</table>

**Peak Optimization Flags (Continued)**

433.milc: basepeak = yes
470.lbm: basepeak = yes
482.sphinx3: basepeak = yes

C++ benchmarks:
444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) 
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -fno-alias -auto-ilp32
-qopt-mem-layout-trans=3

447.dealII: basepeak = yes
450.soplex: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) 
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-malloc-options=3
-qopt-mem-layout-trans=3

453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) 
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -qopt-mem-layout-trans=3

Fortran benchmarks:
410.bwaves: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) 
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-
434.zeusmp: basepeak = yes
437.leslie3d: Same as 410.bwaves
459.GemsFDTD: Same as 410.bwaves

465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) 
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -auto -inline-calloc
-qopt-malloc-options=3

Benchmarks using both Fortran and C:
435.gromacs: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2) 
-par-num-threads=1(pass 1) -qopt-prefetch -auto-ilp32
-qopt-mem-layout-trans=3
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

| SPECfp_rate2006 | 976 |
| SPECfp_rate_base2006 | 960 |

CPU2006 license: 9019  
Test sponsor: Cisco Systems  
Test date: Dec-2017  
Tested by: Cisco Systems  
Hardware Availability: Aug-2017  
Software Availability: Jul-2017

Peak Optimization Flags (Continued)

- 436.cactusADM: basepeak = yes
- 454.calculix: basepeak = yes
- 481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For other inquiries, please contact webmaster@spec.org.

Tested with SPEC CPU2006 v1.2.  
Originally published on 23 February 2018.