Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

SPECfp®2006 = 110
SPECfp_base2006 = 104

Hardware
CPU Name: Intel Xeon Silver 4108
CPU Characteristics: Intel Turbo Boost Technology up to 3.00 GHz
CPU MHz: 1800
FPU: Integrated
CPU(s) enabled: 16 cores, 2 chips, 8 cores/chip
CPU(s) orderable: 1,2 chips
Primary Cache: 32 KB I + 32 KB D on chip per core
Secondary Cache: 1 MB I+D on chip per core

Software
Operating System: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux;
Fortran: Version 17.0.3.191 of Intel Fortran Compiler for Linux
Auto Parallel: Yes
File System: xfs
System State: Run level 3 (multi-user)
### SPEC CFP2006 Result

**Cisco Systems**

Cisco UCS B200 M5 (Intel Xeon Silver 4108, 1.80 GHz)

<table>
<thead>
<tr>
<th>SPECfp2006</th>
<th>110</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECfp_base2006</td>
<td>104</td>
</tr>
</tbody>
</table>

**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems

- **L3 Cache:** 11 MB I+D on chip per chip  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 32/64-bit  
- **Other Cache:** None  
- **Other Software:** None

- **Memory:** 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R, running at 2400)  
- **Disk Subsystem:** 1 x 600 GB SAS HDD, 10K RPM  
- **Other Hardware:** None

**Results Table**

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>410.bwaves</td>
<td>19.2</td>
<td>709</td>
<td>19.4</td>
<td>700</td>
<td>19.7</td>
<td>688</td>
<td>19.2</td>
<td>709</td>
<td>19.4</td>
<td>700</td>
</tr>
<tr>
<td>416.gamess</td>
<td>540</td>
<td>36.3</td>
<td>540</td>
<td>36.2</td>
<td>540</td>
<td>36.3</td>
<td>470</td>
<td>41.6</td>
<td>467</td>
<td>41.9</td>
</tr>
<tr>
<td>433.milc</td>
<td>135</td>
<td>68.0</td>
<td>135</td>
<td>68.2</td>
<td>135</td>
<td>68.0</td>
<td>135</td>
<td>68.0</td>
<td>135</td>
<td>68.0</td>
</tr>
<tr>
<td>434.zeusmp</td>
<td>48.1</td>
<td>189</td>
<td>47.9</td>
<td>190</td>
<td>47.7</td>
<td>191</td>
<td>48.1</td>
<td>189</td>
<td>47.9</td>
<td>190</td>
</tr>
<tr>
<td>435.gromacs</td>
<td>192</td>
<td>37.3</td>
<td>192</td>
<td>37.2</td>
<td>192</td>
<td>37.2</td>
<td>192</td>
<td>37.2</td>
<td>192</td>
<td>37.2</td>
</tr>
<tr>
<td>436.cactusADM</td>
<td>16.1</td>
<td>740</td>
<td>16.1</td>
<td>742</td>
<td>16.1</td>
<td>741</td>
<td>16.1</td>
<td>740</td>
<td>16.1</td>
<td>741</td>
</tr>
<tr>
<td>437.leslie3d</td>
<td>28.5</td>
<td>329</td>
<td>28.3</td>
<td>333</td>
<td>28.1</td>
<td>335</td>
<td>28.5</td>
<td>329</td>
<td>28.3</td>
<td>333</td>
</tr>
<tr>
<td>444.namd</td>
<td>277</td>
<td>28.9</td>
<td>277</td>
<td>28.9</td>
<td>277</td>
<td>28.9</td>
<td>271</td>
<td>29.6</td>
<td>271</td>
<td>29.6</td>
</tr>
<tr>
<td>447.dealII</td>
<td>192</td>
<td>59.7</td>
<td>192</td>
<td>59.4</td>
<td>192</td>
<td>59.5</td>
<td>192</td>
<td>59.7</td>
<td>192</td>
<td>59.9</td>
</tr>
<tr>
<td>450.soplex</td>
<td>209</td>
<td>39.9</td>
<td>210</td>
<td>39.8</td>
<td>210</td>
<td>39.7</td>
<td>209</td>
<td>39.9</td>
<td>210</td>
<td>39.8</td>
</tr>
<tr>
<td>453.povray</td>
<td>94.0</td>
<td>56.6</td>
<td>93.9</td>
<td>56.6</td>
<td>94.2</td>
<td>56.5</td>
<td>83.0</td>
<td>64.1</td>
<td>83.0</td>
<td>64.1</td>
</tr>
<tr>
<td>454.calculix</td>
<td>142</td>
<td>58.3</td>
<td>142</td>
<td>58.3</td>
<td>142</td>
<td>58.1</td>
<td>133</td>
<td>62.3</td>
<td>132</td>
<td>62.5</td>
</tr>
<tr>
<td>459.GemsFDTD</td>
<td>49.4</td>
<td>215</td>
<td>50.1</td>
<td>212</td>
<td>49.5</td>
<td>214</td>
<td>43.5</td>
<td>244</td>
<td>43.8</td>
<td>242</td>
</tr>
<tr>
<td>465.tonto</td>
<td>274</td>
<td>35.9</td>
<td>275</td>
<td>35.8</td>
<td>274</td>
<td>35.9</td>
<td>184</td>
<td>53.5</td>
<td>179</td>
<td>54.9</td>
</tr>
<tr>
<td>470.lbm</td>
<td>15.0</td>
<td>914</td>
<td>15.1</td>
<td>910</td>
<td>15.1</td>
<td>913</td>
<td>15.0</td>
<td>914</td>
<td>15.1</td>
<td>910</td>
</tr>
<tr>
<td>481.wrf</td>
<td>127</td>
<td>88.1</td>
<td>133</td>
<td>83.9</td>
<td>126</td>
<td>88.4</td>
<td>127</td>
<td>88.1</td>
<td>133</td>
<td>83.9</td>
</tr>
<tr>
<td>482.sphinx3</td>
<td>403</td>
<td>48.4</td>
<td>404</td>
<td>48.2</td>
<td>407</td>
<td>47.8</td>
<td>403</td>
<td>48.4</td>
<td>404</td>
<td>48.2</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

- **BIOS Settings:**
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise
  - Power Performance Tuning set to OS Controls
  - SNC set to Disabled
  - Patrol Scrub set to Disabled
- **Sysinfo program:** 
  `/home/cpu2006-1.2/config/sysinfo.rev6993`
- **Revision:** 6993 of 2015-11-06
- **Running:** on `linux-djj4 Sun Dec 17 04:31:20 2017`

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Platform Notes (Continued)

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4108 CPU @ 1.80GHz
2 "physical id"s (chips)
16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7
cache size : 11264 KB

From /proc/meminfo
MemTotal:       394667604 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 4 06:54

SPEC is set to: /home/cpu2006-1.2
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 559G 129G 430G 24% /

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

reads system data which is "intended to allow hardware to be accurately 
determined", but the intent may not be met, as there are frequent changes to 
hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
  24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz, configured at 2400 MHz

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "16"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM 
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/transparent_hugepage/enabled
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) 
is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) 
is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) 
is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on 
past performance using the historical hardware and/or 
software described on this result page.

The system as described on this result page was formerly 
generally available. At the time of this publication, it may 
not be shipping, and/or may not be supported, and/or may fail 
to meet other tests of General Availability described in the 

This measured result may not be representative of the result 
that would be measured were this benchmark run with hardware 
and software available as of the publication date.

Base Compiler Invocation

C benchmarks:
  icc -m64

C++ benchmarks:
  icpc -m64

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Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.sphinx3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch

Peak Compiler Invocation

C benchmarks:
icc -m64

Continued on next page
Peak Compiler Invocation (Continued)

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Benchmarks using both Fortran and C:
  icc -m64 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
  433.milc: basepeak = yes
  470.lbm: basepeak = yes
  482.sphinx3: basepeak = yes

C++ benchmarks:
  444.namd: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -fno-alias -auto-ilp32
  447.dealII: basepeak = yes
  450.soplex: basepeak = yes
  453.povray: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -unroll4 -ansi-alias

Fortran benchmarks:
  410.bwaves: basepeak = yes
  416.gamess: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
    -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
    -no-prec-div(pass 2) -unroll2 -inline-level=0 -scalar-rep-
## Peak Optimization Flags (Continued)

434.zeusmp: basepeak = yes
437.leslie3d: basepeak = yes

459.GemsFDTD: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -inline-level=0
-qopt-prefetch -parallel

465.tonto: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -inline-callloc -qopt-malloc-options=3
-auto -unroll4

Benchmarks using both Fortran and C:
435.gromacs: basepeak = yes
436.cactusADM: basepeak = yes
454.calculix: -xCORE-AVX2 -ipo -O3 -no-prec-div -auto-1lp32
481.wrf: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml