## SPECint® CINT2006 Result

**Cisco Systems**  
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)  

<table>
<thead>
<tr>
<th>SPECint_rate2006</th>
<th>1160</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint_rate_base2006</td>
<td>1100</td>
</tr>
</tbody>
</table>

**CPU2006 license:** 9019  
**Test sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Hardware Availability:** Aug-2017  
**Software Availability:** Jul-2017  
**Test date:** Dec-2017

### Hardware

<table>
<thead>
<tr>
<th>Component</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Gold 6134M</td>
</tr>
<tr>
<td>CPU Characteristics</td>
<td>Intel Turbo Boost Technology up to 3.70 GHz</td>
</tr>
<tr>
<td>CPU MHZ</td>
<td>3200</td>
</tr>
<tr>
<td>FPU</td>
<td>Integrated</td>
</tr>
<tr>
<td>CPU(s) enabled</td>
<td>16 cores, 2 chips, 8 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td>CPU(s) orderable</td>
<td>1.2 chips</td>
</tr>
<tr>
<td>Primary Cache</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Secondary Cache</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3 Cache</td>
<td>24.75 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other Cache</td>
<td>None</td>
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<tr>
<td>Memory</td>
<td>384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Disk Subsystem</td>
<td>1 x 600 GB SAS HDD, 10K RPM</td>
</tr>
<tr>
<td>Other Hardware</td>
<td>None</td>
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### Software

<table>
<thead>
<tr>
<th>Component</th>
<th>Details</th>
</tr>
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<tbody>
<tr>
<td>Operating System</td>
<td>SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran Compiler</td>
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<tr>
<td>Auto Parallel</td>
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<tr>
<td>File System</td>
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<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers</td>
<td>32-bit</td>
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<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
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<tr>
<td>Other Software</td>
<td>Microquill SmartHeap V10.2</td>
</tr>
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### Test Results

<table>
<thead>
<tr>
<th>SPEC Benchmark</th>
<th>CINT2006 copies</th>
<th>SPECint_rate2006</th>
<th>SPECint_rate_base2006</th>
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<tr>
<td>401.bzip2</td>
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<td>403.gcc</td>
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<td>404</td>
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<tr>
<td>429.mcf</td>
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<td>801</td>
<td>656</td>
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<tr>
<td>456.hmmer</td>
<td>32</td>
<td>741</td>
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<td>458.sjeng</td>
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<tr>
<td>464.h264ref</td>
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<td>1160</td>
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<tr>
<td>471.omnetpp</td>
<td>32</td>
<td>543</td>
<td>495</td>
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<tr>
<td>473.astar</td>
<td>32</td>
<td>610</td>
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<tr>
<td>483.xalancbmk</td>
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SPEClint_rate2006 = 1160  
SPEClint_rate_base2006 = 1100
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

SPECint_rate2006 = 1160
SPECint_rate_base2006 = 1100

Results Table

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<table>
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<td>1360</td>
<td>163</td>
<td>1350</td>
<td>162</td>
<td>1360</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux Mon Dec 18 20:22:17 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6134M CPU @ 3.20GHz

Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

| SPECint_rate2006  = | 1160 |
| SPECint_rate_base2006  = | 1100 |

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

| Test date:       | Dec-2017 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Jul-2017 |

Platform Notes (Continued)

2 "physical id"s (chips)
32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
physical 0: cores 0 2 3 9 16 19 26 27
physical 1: cores 0 2 3 9 16 19 26 27
cache size : 25344 KB

From /proc/meminfo
MemTotal: 394667540 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID=sles
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 31 19:31

SPEC is set to: /home/cpu2006-1.2

<table>
<thead>
<tr>
<th>Filesystem</th>
<th>Type</th>
<th>Size</th>
<th>Used</th>
<th>Avail</th>
<th>Use%</th>
<th>Mounted on</th>
</tr>
</thead>
<tbody>
<tr>
<td>/dev/sda1</td>
<td>xfs</td>
<td>280G</td>
<td>146G</td>
<td>135G</td>
<td>53%</td>
<td>/</td>
</tr>
</tbody>
</table>

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
Memory:
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPECint_rate2006 = 1160
SPECint_rate_base2006 = 1100

CPU2006 license: 9019
Test date: Dec-2017
Test sponsor: Cisco Systems
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Platform Notes (Continued)

(End of data from sysinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/intel/lib/ia32:/opt/intel/lib/intel64:/home/cpu2006-1.2/sh10.2"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
Filesystem page cache cleared with:
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Base Compiler Invocation

C benchmarks:
icc -m32 -L/opt/intel/lib/ia32

C++ benchmarks:
icpc -m32 -L/opt/intel/lib/ia32
## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

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**CPU2006 license:** 9019  
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### Base Portability Flags

- 400.perlbench: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32`
- 401.bzip2: `-D_FILE_OFFSET_BITS=64`
- 403.gcc: `-D_FILE_OFFSET_BITS=64`
- 429.mcf: `-D_FILE_OFFSET_BITS=64`
- 445.gobmk: `-D_FILE_OFFSET_BITS=64`
- 456.hmmer: `-D_FILE_OFFSET_BITS=64`
- 458.sjeng: `-D_FILE_OFFSET_BITS=64`
- 462.libquantum: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`
- 464.h264ref: `-D_FILE_OFFSET_BITS=64`
- 471.omnetpp: `-D_FILE_OFFSET_BITS=64`
- 473.astar: `-D_FILE_OFFSET_BITS=64`
- 483.xalancbmk: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`

### Base Optimization Flags

**C benchmarks:**

- `-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3`

**C++ benchmarks:**

- `-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3`
- `-Wl,-z,muldefs -L/home/cpu2006-1.2/sh10.2 -lsmartheap`

### Base Other Flags

**C benchmarks:**

- `403.gcc: -Dalloca=_alloca`

### Peak Compiler Invocation

**C benchmarks (except as noted below):**

- `icc -m32 -L/opt/intel/lib/ia32`
- `icc -m64`
- `icc -m64`
- `icc -m64`
- `icc -m64`

**C++ benchmarks:**

- `icpc -m32 -L/opt/intel/lib/ia32`
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

SPEC CINT2006 Result

SPECint_rate2006 = \(1160\)
SPECint_rate_base2006 = \(1100\)

CPU2006 license: 9019
Test sponsor: Cisco Systems
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CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Portability Flags

400.perlbench: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
-qopt-mem-layout-trans=3

403.gcc: -xHOST -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3

429.mcf: basepeak = yes

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-mem-layout-trans=3

456.hmmer: -xHOST -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
-qopt-mem-layout-trans=3

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll4 -auto-ilp32
-qopt-mem-layout-trans=3

462.libquantum: basepeak = yes

464.h264ref: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3

Continued on next page
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Cisco UCS B200 M5 (Intel Xeon Gold 6134M, 3.20 GHz)

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CPU2006 license: 9019
Test sponsor: Cisco Systems
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Test date: Dec-2017
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Software Availability: Jul-2017

Peak Optimization Flags (Continued)

C++ benchmarks:

471.omnetpp: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
   -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
   -no-prec-div(pass 2)
   -qopt-ra-region-strategy=block
   -qopt-mem-layout-trans=3 -Wl,-z,muldefs
   -L/home/cpu2006-1.2/sh10.2 -lsmartheap

473.astar: basepeak = yes
483.xalancbmk: basepeak = yes

Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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