**Cisco Systems**

**Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)**

**SPEClnt\_rate2006 = 1570**

**SPEClnt\_rate\_base2006 = 1490**

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System:</td>
<td>CPU Name: Intel Xeon Gold 6136</td>
</tr>
<tr>
<td>Compiler:</td>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz</td>
</tr>
<tr>
<td>Fortran: Compiler for Linux:</td>
<td>CPU MHz: 3000</td>
</tr>
<tr>
<td>Auto Parallel:</td>
<td>CPU(s) enabled: 24 cores, 2 chips, 12 cores/chip, 2 threads/core</td>
</tr>
<tr>
<td>File System:</td>
<td>CPU(s) orderable: 1,2 chips</td>
</tr>
<tr>
<td>System State:</td>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>Secondary Cache: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>L3 Cache: 24.75 MB I+D on chip per core</td>
</tr>
<tr>
<td>Other Software:</td>
<td>Other Cache: None</td>
</tr>
<tr>
<td>Microquill SmartHeap V10.2</td>
<td>Memory: 384 GB (24 x 16 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td></td>
<td>Disk Subsystem: 1 x 600 GB SAS HDD, 10K RPM</td>
</tr>
</tbody>
</table>

**Test date:** Dec-2017  
**Hardware Availability:** Aug-2017  
**Software Availability:** Jul-2017
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

### Results Table

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<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>710</td>
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<td>709</td>
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<td>372</td>
<td>1040</td>
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<td>462.libquantum</td>
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<td>36.4</td>
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<td>464.h264ref</td>
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<td>654</td>
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<td>471.omnetpp</td>
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<td>473.astar</td>
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<td>408</td>
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<td>823</td>
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<tr>
<td>483.xalancbmk</td>
<td>48</td>
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<td>1680</td>
<td>196</td>
<td>1690</td>
<td>197</td>
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<td>1680</td>
<td>196</td>
<td>1690</td>
<td>197</td>
<td>1680</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on linux-mys2 Thu Dec 7 00:00:23 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6136 CPU @ 3.00GHz
								
Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECint_rate2006 = 1570
SPECint_rate_base2006 = 1490

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

2 "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpts from /proc/cpuinfo might not be reliable. Use with
cautions.)
cpu cores : 12
siblings : 24
physical 0: cores 0 1 2 3 4 8 9 11 17 18 19 20
physical 1: cores 0 1 4 9 10 11 17 18 24 25 26 27

cache size : 25344 KB

From /proc/meminfo
MemTotal: 394831836 KB
HugePages_Total: 0
Hugepagesize: 2048 KB

/usr/bin/lsb_release -d
SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
SuSE-release:
  SUSE Linux Enterprise Server 12 (x86_64)
  VERSION = 12
  PATCHLEVEL = 2
  # This file is deprecated and will be removed in a future service pack or
  release.
  # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID=sles"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
(9464f67) x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 1 20:36

SPEC is set to: /home/cpu2006-1.2

Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program
reads system data which is "intended to allow hardware to be accurately
determined", but the intent may not be met, as there are frequent changes to
hardware, firmware, and the "DMTF SMBIOS" standard.

Continued on next page
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

**SPECint_rate2006** = 1570
**SPECint_rate_base2006** = 1490

<table>
<thead>
<tr>
<th>CPU2006 license</th>
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<td>9019</td>
<td>Dec-2017</td>
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<thead>
<tr>
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<td>Aug-2017</td>
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<table>
<thead>
<tr>
<th>Tested by</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Cisco Systems</td>
<td>Jul-2017</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

**BIOS** Cisco Systems, Inc. B200M5.3.2.1d.5.0727171353 07/27/2017
**Memory:**
24x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

(End of data from sysinfo program)

**General Notes**

Environment variables set by runspec before the start of the run:
```
LD_LIBRARY_PATH = */opt/intel/compilers_and_libraries_2018.0.128/linux/compiler/lib/ia32:/opt/intel/compilers_and_libraries_2018.0.128/linux/compiler/lib/intel64:/home/cpu2006-1.2/sh10.2
```

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
```
echo always > /sys/kernel/mm/transparent_hugepage/enabled
```
Filesystem page cache cleared with:
```
shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
```
runcspec command invoked through numactl i.e.:
```
umactl --interleave=all runspec <etc>
```
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

**Base Compiler Invocation**

C benchmarks:
```
icc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32
```

C++ benchmarks:
```
icpc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32
```
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECint_rate2006 = 1570
SPECint_rate_base2006 = 1490

CPU2006 license: 9019
Test date: Dec-2017
Test sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Jul-2017

Base Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -D_FILE_OFFSET_BITS=64
403.gcc: -D_FILE_OFFSET_BITS=64
429.mcf: -D_FILE_OFFSET_BITS=64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -D_FILE_OFFSET_BITS=64
458.sjeng: -D_FILE_OFFSET_BITS=64
462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
464.h264ref: -D_FILE_OFFSET_BITS=64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -D_FILE_OFFSET_BITS=64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Base Optimization Flags

C benchmarks:
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3

C++ benchmarks:
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
-Wl,-z,muldefs -L/home/cpu2006-1.2/sh10.2 -lsmartheap

Base Other Flags

C benchmarks:
403.gcc: -Dalloca=_alloca

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32

400.perlbench: icc -m64
401.bzip2: icc -m64
456.hmmer: icc -m64
458.sjeng: icc -m64

C++ benchmarks:
icpc -m32 -L/opt/intel/compilers_and_libraries_2018.0.128/linux/lib/ia32
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

SPECint\_rate2006 = \textbf{1570}
SPECint\_rate\_base2006 = \textbf{1490}

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems
Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: Jul-2017

### Peak Portability Flags

- **400.perlbench**: -DSPEC\_CPU\_LP64 -DSPEC\_CPU\_LINUX\_X64
- **401.bzip2**: -DSPEC\_CPU\_LP64
- **403.gcc**: -D\_FILE\_OFFSET\_BITS=64
- **429.mcf**: -D\_FILE\_OFFSET\_BITS=64
- **445.gobmk**: -D\_FILE\_OFFSET\_BITS=64
- **456.hmmer**: -DSPEC\_CPU\_LP64
- **458.sjeng**: -DSPEC\_CPU\_LP64
- **462.libquantum**: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX
- **464.h264ref**: -D\_FILE\_OFFSET\_BITS=64
- **471.omnetpp**: -D\_FILE\_OFFSET\_BITS=64
- **473.astar**: -D\_FILE\_OFFSET\_BITS=64
- **483.xalancbmk**: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_CPU\_LINUX

### Peak Optimization Flags

C benchmarks:

- **400.perlbench**: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -auto-ilp32 -qopt-mem-layout-trans=3

- **401.bzip2**: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -qopt-prefetch -auto-ilp32
  -qopt-mem-layout-trans=3

- **403.gcc**: -xHOST -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3

- **429.mcf**: basepeak = yes

- **445.gobmk**: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -qopt-mem-layout-trans=3

- **456.hmmer**: -xHOST -ipo -O3 -no-prec-div -unroll2 -auto-ilp32
  -qopt-mem-layout-trans=3

- **458.sjeng**: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -unroll4 -auto-ilp32
  -qopt-mem-layout-trans=3

- **462.libquantum**: basepeak = yes

- **464.h264ref**: -prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)
  -par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
  -no-prec-div(pass 2) -unroll2 -qopt-mem-layout-trans=3
## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6136, 3.00 GHz)

| SPECint_rate2006 = | 1570 |
| SPECint_rate_base2006 = | 1490 |

| CPU2006 license: | 9019 |
| Test sponsor: | Cisco Systems |
| Tested by: | Cisco Systems |
| Test date: | Dec-2017 |
| Hardware Availability: | Aug-2017 |
| Software Availability: | Jul-2017 |

### Peak Optimization Flags (Continued)

**C++ benchmarks:**

- 471.omnetpp: `-prof-gen(pass 1) -prof-use(pass 2) -xHOST(pass 2)`
- `-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)`
- `-no-prec-div(pass 2)`
- `-qopt-ra-region-strategy=block`
- `-qopt-mem-layout-trans=3 -W1,-z,muldefs`
- `-L/home/cpu2006-1.2/sh10.2 -lsmartheap`

```
473.astar: basepeak = yes
483.xalancbmk: basepeak = yes
```

### Peak Other Flags

**C benchmarks:**

- 403.gcc: `-Dalloca=_alloca`

The flags files that were used to format this result can be browsed at:

- [Intel ic17.0-official-linux64-revF.html](http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html)
- [Cisco Platform Settings V1.2-revH.html](http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html)

You can also download the XML flags sources by saving the following links:

- [Intel ic17.0-official-linux64-revF.xml](http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml)
- [Cisco Platform Settings -V1.2-revH.xml](http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml)

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For other inquiries, please contact webmaster@spec.org.

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