## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6138, 2.00 GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating System: Red Hat Enterprise Linux Server release 7.3 (Maipo) 3.10.0-514.el7.x86_64</td>
<td>CPU Name: Intel Xeon Gold 6138</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 17.0.3.191 of Intel C/C++ Compiler for Linux</td>
<td>CPU Characteristics: Intel Turbo Boost Technology up to 3.70 GHz</td>
</tr>
<tr>
<td>Auto Parallel: Yes</td>
<td>CPU MHZ: 2000</td>
</tr>
<tr>
<td>File System: xfs</td>
<td>FPU: Integrated</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>CPU(s) enabled: 80 cores, 4 chips, 20 cores/chip</td>
</tr>
<tr>
<td>Base Pointers: 32/64-bit</td>
<td>CPU(s) orderable: 2,4 chips</td>
</tr>
<tr>
<td>Peak Pointers: 32/64-bit</td>
<td>Primary Cache: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Other Software: Microquill SmartHeap V10.2</td>
<td>Secondary Cache: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td></td>
<td>L3 Cache: 27.5 MB I+D on chip per chip</td>
</tr>
</tbody>
</table>

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### SPECint<sub>2006</sub> = 79.7

### SPECint<sub>base2006</sub> = 76.2
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6138, 2.00 GHz)

SPECint2006 = 79.7
SPECint_base2006 = 76.2

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<tr>
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<td>46.9</td>
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<td>46.7</td>
<td>210</td>
<td>46.6</td>
<td>184</td>
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<td>184</td>
<td>53.1</td>
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<td>403.mcf</td>
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<td>43.7</td>
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<td>45.3</td>
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<td>45.1</td>
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<td>78.4</td>
<td>113</td>
<td>80.8</td>
<td>115</td>
<td>79.1</td>
<td>117</td>
<td>77.8</td>
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<tr>
<td>456.hmmer</td>
<td>96.4</td>
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<td>96.6</td>
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<td>458.sjeng</td>
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<td>37.2</td>
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<td>38.0</td>
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<td>462.libquantum</td>
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<td>2.58</td>
<td>8040</td>
<td>2.53</td>
<td>8190</td>
<td>2.52</td>
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<td>8040</td>
<td>2.53</td>
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<td>38.7</td>
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<tr>
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<td>77.4</td>
<td>89.2</td>
<td>76.9</td>
<td>89.7</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The config file option 'submit' was used.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2006-1.2/config/sysinfo.rev6993
Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
running on Plumas2-127.128 Thu Dec 14 08:21:46 2017

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see:
http://www.spec.org/cpu2006/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6138 CPU @ 2.00GHz
  4 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
Continued on next page
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6138, 2.00 GHz)

SPECint2006 = 79.7
SPECint_base2006 = 76.2

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: May-2017

Platform Notes (Continued)

following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 2: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 3: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
cache size : 28160 KB

From /proc/meminfo
MemTotal: 790981380 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="Red Hat Enterprise Linux Server"
VERSION="7.3 (Maipo)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="7.3"
PRETTY_NAME=OpenStack
ANSI_COLOR="0;31"
CPE_NAME="cpe:/o:redhat:enterprise_linux:7.3:GA:server"
redhat-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)
system-release: Red Hat Enterprise Linux Server release 7.3 (Maipo)

uname -a:
Linux Plumas2-127.128 3.10.0-514.el7.x86_64 #1 SMP Wed Oct 19 11:24:13 EDT 2016 x86_64 x86_64 x86_64 GNU/Linux
run-level 3 Jan 13 06:44

SPEC is set to: /home/cpu2006-1.2
Additional information from dmidecode:

Warning: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017 Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
Memory:
96x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

The correct amount of Memory installed is 768 GB (48 x 16 GB)

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SPEC CINT2006 Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6138, 2.00 GHz)

SPECint2006 = 79.7
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CPU2006 license: 9019
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Platform Notes (Continued)

and the dmidecode is reporting invalid number of DIMMs installed
Installed Memory:
48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

General Notes

Environment variables set by runspec before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2006-1.2/lib/ia32:/home/cpu2006-1.2/lib/intel64:/home/cpu2006-1.2/sh10.2"
OMP_NUM_THREADS = "80"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.2
Transparent Huge Pages enabled with:
echo always > /sys/kernel/mm/transparent_hugepage/enabled
No: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
No: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

This benchmark result is intended to provide perspective on past performance using the historical hardware and/or software described on this result page.

The system as described on this result page was formerly generally available. At the time of this publication, it may not be shipping, and/or may not be supported, and/or may fail to meet other tests of General Availability described in the SPEC OSG Policy document, http://www.spec.org/osg/policy.html

This measured result may not be representative of the result that would be measured were this benchmark run with hardware and software available as of the publication date.

Base Compiler Invocation

C benchmarks:
  icc -m64

C++ benchmarks:
  icpc -m64
## Base Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>400.perlbench</td>
<td>-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64</td>
</tr>
<tr>
<td>401.bzip2</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>403.gcc</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>429.mcf</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>445.gobmk</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>456.hmmer</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>458.sjeng</td>
<td>-DSPEC_CPU_LP64</td>
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<tr>
<td>462.libquantum</td>
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<td>473.astar</td>
<td>-DSPEC_CPU_LP64</td>
</tr>
<tr>
<td>483.xalancbmk</td>
<td>-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX</td>
</tr>
</tbody>
</table>

## Base Optimization Flags

### C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -parallel -qopt-prefetch -auto-p32

### C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -auto-p32 -Wl,-z,muldefs -L/sh10.2 -lsmartheap64

## Base Other Flags

### C benchmarks:
403.gcc: -Dalloca=_alloca

## Peak Compiler Invocation

### C benchmarks (except as noted below):
```bash
icc -m64
dir2bench: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
445.gobmk: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```

### C++ benchmarks (except as noted below):
```bash
icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
dir2bench: icc -m64
445.gobmk: icc -m32 -L/opt/intel/compilers_and_libraries_2017/linux/lib/ia32
```
SPEC CINT2006 Result

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Cisco UCS C480 M5 (Intel Xeon Gold 6138, 2.00 GHz)

SPECint2006 = 79.7
SPECint_base2006 = 76.2

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Dec-2017
Hardware Availability: Aug-2017
Software Availability: May-2017

Peak Portability Flags

400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
401.bzip2: -DSPEC_CPU_LP64
403.gcc: -DSPEC_CPU_LP64
429.mcf: -DSPEC_CPU_LP64
445.gobmk: -D_FILE_OFFSET_BITS=64
456.hmmer: -DSPEC_CPU_LP64
458.sjeng: -DSPEC_CPU_LP64
462.libquantum: -DSPEC_CPU_LP64 -DSPEC_CPU_LINUX
464.h264ref: -DSPEC_CPU_LP64
471.omnetpp: -D_FILE_OFFSET_BITS=64
473.astar: -DSPEC_CPU_LP64
483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX

Peak Optimization Flags

C benchmarks:

400.perlbench: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -qopt-prefetch

401.bzip2: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div -auto-ilp32 -qopt-prefetch

403.gcc: -xCORE-AVX2 -ipo -O3 -no-prec-div -inline-cALLOC
-qopt-malloc-options=3 -auto-ilp32

429.mcf: -xCORE-AVX2 -ipo -O3 -no-prec-div -parallel
-qopt-prefetch -auto-p32

445.gobmk: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2)

456.hmmer: basepeak = yes

458.sjeng: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX2(pass 2)
-par-num-threads=1(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -unroll14

462.libquantum: basepeak = yes

464.h264ref: basepeak = yes

C++ benchmarks:

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Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6138, 2.00 GHz)

| SPECint2006 | 79.7 |
| SPECint_base2006 | 76.2 |

**CPU2006 license:** 9019  
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**Hardware Availability:** Aug-2017  
**Software Availability:** May-2017

**Peak Optimization Flags (Continued)**

471.omnetpp: 
- prof-gen(pass 1)  
- prof-use(pass 2)  
- xCORE-AVX2(pass 2)  
- par-num-threads=1(pass 1)  
- ipo(pass 2)  
- O3(pass 2)  
- no-prec-div(pass 2)  
- qopt-ra-region-strategy=block  
- Wl,-z,muldefs -L/sh10.2 -lsmartheap

473.astar: 
- xCORE-AVX2  
- ipo -O3 -no-prec-div -qopt-prefetch  
- auto-p32 -Wl,-z,muldefs -L/sh10.2 -lsmartheap64

483.xalancbmk: 
- xCORE-AVX2  
- ipo -O3 -no-prec-div -qopt-prefetch  
- Wl,-z,muldefs -L/sh10.2 -lsmartheap

**Peak Other Flags**

C benchmarks: 

403.gcc: -Dalloca=_alloca

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester.  
For other inquiries, please contact webmaster@spec.org.

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