Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6140, 2.30GHz)

**SPECspeed**
- SPECspeed\(^\text{\textregistered}2017\_fp\_base\) = 142
- SPECspeed\(^\text{\textregistered}2017\_fp\_peak\) = 144

**CPU2017 License**: 9019
**Test Date**: Oct-2017
**Test Sponsor**: Cisco Systems
**Hardware Availability**: Aug-2017
**Tested by**: Cisco Systems
**Software Availability**: Sep-2017

### Threads

| 603.bwaves_s | 72 threads | SPECspeed\(^\text{\textregistered}2017\_fp\_base\) = 142 |
| 607.cactuBSSN_s | 72 threads | SPECspeed\(^\text{\textregistered}2017\_fp\_peak\) = 144 |
| 619.lbm_s | 72 threads |
| 621.wrf_s | 72 threads |
| 627.cam4_s | 72 threads |
| 628.pop2_s | 72 threads |
| 638.imagick_s | 72 threads |
| 644.nab_s | 72 threads |
| 649.fotonik3d_s | 72 threads |
| 654.roms_s | 72 threads |

### Hardware

- **CPU Name**: Intel Xeon Gold 6140
- **Max MHz**: 3700
- **Nominal**: 2300
- **Enabled**: 72 cores, 4 chips
- **Orderable**: 2,4 Chips
- **Cache L1**: 32 KB I + 32 KB D on chip per core
- **L2**: 1 MB I+D on chip per core
- **L3**: 24.75 MB I+D on chip per chip
- **Memory**: 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage**: 1 x 1 TB SAS HDD, 7.2K RPM
- **Other**: None

### Software

- **OS**: SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
- **Compiler**: C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel**: Yes
- **Firmware**: Version 3.1.0 released May-2017
- **File System**: xfs
- **System State**: Run level 5 (multi-user)
- **Base Pointers**: 64-bit
- **Peak Pointers**: 64-bit
- **Other**: None
- **Power Management**: --
Cisco Systems
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SPECspeed®2017_fp_base = 142
SPECspeed®2017_fp_peak = 144

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
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<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>72</td>
<td>70.9</td>
<td>832</td>
<td>72.2</td>
<td>818</td>
<td>72.1</td>
<td>818</td>
<td>72</td>
<td>71.1</td>
<td>830</td>
<td>71.9</td>
<td>820</td>
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<td>824</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>72</td>
<td>85.8</td>
<td>194</td>
<td>83.9</td>
<td>199</td>
<td>84.1</td>
<td>198</td>
<td>72</td>
<td>83.7</td>
<td>199</td>
<td>83.8</td>
<td>199</td>
<td>83.6</td>
<td>199</td>
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<tr>
<td>619.lbm_s</td>
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<td>65.7</td>
<td>79.7</td>
<td>65.6</td>
<td>79.8</td>
<td>65.4</td>
<td>80.1</td>
<td>72</td>
<td>65.8</td>
<td>79.6</td>
<td>65.4</td>
<td>80.1</td>
<td>65.6</td>
<td>79.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>72</td>
<td>211</td>
<td>62.6</td>
<td>215</td>
<td>61.4</td>
<td>207</td>
<td>64.0</td>
<td>72</td>
<td>202</td>
<td>65.4</td>
<td>205</td>
<td>64.6</td>
<td>207</td>
<td>64.0</td>
<td></td>
<td></td>
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<tr>
<td>627.cam4_s</td>
<td>72</td>
<td>74.7</td>
<td>119</td>
<td>74.5</td>
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<td>75.1</td>
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<td>72</td>
<td>74.8</td>
<td>119</td>
<td>74.8</td>
<td>118</td>
<td>74.8</td>
<td>118</td>
<td></td>
<td></td>
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<tr>
<td>628.pop2_s</td>
<td>72</td>
<td>223</td>
<td>53.3</td>
<td>235</td>
<td>50.6</td>
<td>226</td>
<td>52.5</td>
<td>72</td>
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<td>224</td>
<td>53.0</td>
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<td></td>
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<tr>
<td>638.imagick_s</td>
<td>72</td>
<td>84.0</td>
<td>172</td>
<td>81.9</td>
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<td>82.1</td>
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<td>72</td>
<td>84.8</td>
<td>170</td>
<td>82.0</td>
<td>176</td>
<td>83.4</td>
<td>173</td>
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<tr>
<td>644.nab_s</td>
<td>72</td>
<td>54.9</td>
<td>318</td>
<td>55.0</td>
<td>318</td>
<td>55.0</td>
<td>318</td>
<td>72</td>
<td>55.0</td>
<td>318</td>
<td>54.7</td>
<td>319</td>
<td>55.0</td>
<td>317</td>
<td></td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>72</td>
<td>92.4</td>
<td>98.7</td>
<td>89.7</td>
<td>102</td>
<td>87.5</td>
<td>104</td>
<td>72</td>
<td>89.5</td>
<td>102</td>
<td>90.0</td>
<td>101</td>
<td>88.4</td>
<td>103</td>
<td></td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>72</td>
<td>129</td>
<td>122</td>
<td>131</td>
<td>120</td>
<td>137</td>
<td>115</td>
<td>72</td>
<td>123</td>
<td>128</td>
<td>118</td>
<td>113</td>
<td>133</td>
<td>121</td>
<td>130</td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32;/home/cpu2017/lib/intel64;/home/cpu2017/je5.0.1-32;/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4 Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)
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<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Oct-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Sep-2017</td>
</tr>
</tbody>
</table>

**SPEC CPU®2017 Floating Point Speed Result**

**SPECspeed®2017_fp_base = 142**

**SPECspeed®2017_fp_peak = 144**

Platform Notes (Continued)

running on linux–g4fl Sat Sep 30 11:18:40 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>model name</td>
<td>Intel(R) Xeon(R) Gold 6140 CPU @ 2.30GHz</td>
</tr>
<tr>
<td>4 &quot;physical id&quot;s (chips)</td>
<td></td>
</tr>
<tr>
<td>72 &quot;processors&quot;</td>
<td></td>
</tr>
<tr>
<td>cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)</td>
<td></td>
</tr>
<tr>
<td>cpu cores</td>
<td>18</td>
</tr>
<tr>
<td>siblings</td>
<td>18</td>
</tr>
<tr>
<td>physical 0: cores</td>
<td>0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27</td>
</tr>
<tr>
<td>physical 1: cores</td>
<td>0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27</td>
</tr>
<tr>
<td>physical 2: cores</td>
<td>0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27</td>
</tr>
<tr>
<td>physical 3: cores</td>
<td>0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27</td>
</tr>
</tbody>
</table>

From lscpu:

<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture:</td>
<td>x86_64</td>
</tr>
<tr>
<td>CPU op-mode(s):</td>
<td>32-bit, 64-bit</td>
</tr>
<tr>
<td>Byte Order:</td>
<td>Little Endian</td>
</tr>
<tr>
<td>CPU(s):</td>
<td>72</td>
</tr>
<tr>
<td>On-line CPU(s) list:</td>
<td>0-71</td>
</tr>
<tr>
<td>Thread(s) per core:</td>
<td>1</td>
</tr>
<tr>
<td>Core(s) per socket:</td>
<td>18</td>
</tr>
<tr>
<td>Socket(s):</td>
<td>4</td>
</tr>
<tr>
<td>NUMA node(s):</td>
<td>4</td>
</tr>
<tr>
<td>Vendor ID:</td>
<td>GenuineIntel</td>
</tr>
<tr>
<td>CPU family:</td>
<td>6</td>
</tr>
<tr>
<td>Model:</td>
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</tr>
<tr>
<td>Model name:</td>
<td>Intel(R) Xeon(R) Gold 6140 CPU @ 2.30GHz</td>
</tr>
<tr>
<td>Stepping:</td>
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<tr>
<td>CPU MHz:</td>
<td>1191.342</td>
</tr>
<tr>
<td>CPU max MHz:</td>
<td>3700.0000</td>
</tr>
<tr>
<td>CPU min MHz:</td>
<td>1000.0000</td>
</tr>
<tr>
<td>BogoMIPS:</td>
<td>4600.20</td>
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<tr>
<td>Virtualization:</td>
<td>VT-x</td>
</tr>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
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<tr>
<td>L2 cache:</td>
<td>1024K</td>
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<tr>
<td>L3 cache:</td>
<td>25344K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-17</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>18-35</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>36-53</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>54-71</td>
</tr>
</tbody>
</table>
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| SPECspeed®2017_fp_base | 142 |
| SPECspeed®2017_fp_peak | 144 |

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2017
Hardware Availability: Aug-2017
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Platform Notes (Continued)

Flags:                  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtrr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abtm 3nowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_apicreq intel_pt tpr_shadow vmx flexpriority ept vpid
fsqsb fsgsbase tsc_adjust bni hle avx2 smep bmi2 3dnow invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

/proc/cpuinfo cache data
  cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
  node 0 size: 192015 MB
  node 0 free: 191901 MB
  node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
  node 1 size: 193521 MB
  node 1 free: 193404 MB
  node 2 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
  node 2 size: 193521 MB
  node 2 free: 190502 MB
  node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
  node 3 size: 193372 MB
  node 3 free: 191524 MB
  node distances:
    node 0 1 2 3
    0: 10 21 21 31
    1: 21 10 31 21
    2: 21 31 10 21
    3: 31 21 21 10

From /proc/meminfo
  MemTotal:  790968500 kB
  HugePages_Total:       0
  Hugepagesize:  2048 kB

/usr/bin/lsb_release -d
  SUSE Linux Enterprise Server 12 SP2

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)

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Platform Notes (Continued)

VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-g4f1 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux
run-level 5 Oct 30 02:43

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda6 xfs 871G 50G 821G 6% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017
  Memory: 48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base, peak)
==============================================================================

icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
==============================================================================

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Compiler Version Notes (Continued)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
                | 654.roms_s(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                | 628.pop2_s(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: –DSPEC_LP64

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Base Portability Flags (Continued)

607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div
-ipt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

(Continued on next page)
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</tbody>
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Base Other Flags (Continued)

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

Peak Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
619.ibm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2
-qopt-prefetch -mtune=skylake -ffinite-math-only -ipo
-03 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP

638.imagick_s: -xCORE-AVX2 -mtune=skylake -ipo -03 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3
-qopenmp -DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:
-prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6140, 2.30GHz)

SPECspeed®2017_fp_base = 142
SPECspeed®2017_fp_peak = 144

CPU2017 License: 9019
Test Date: Oct-2017
Test Sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Sep-2017

Peak Optimization Flags (Continued)

Fortran benchmarks (continued):
-DSPEC_OPENMP -O2 -xCORE-AVX2 -qopt-prefetch -mtune=skylake
-ffinite-math-only -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3
-qopenmp -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2
-qopt-prefetch -mtune=skylake -ffinite-math-only -ipo
-O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

627.cam4_s: -xCORE-AVX2 -mtune=skylake -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=3
-qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX2 -qopt-prefetch
-mtune=skylake -ffinite-math-only -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6140, 2.30GHz)  
SPECspeed®2017_fp_base = 142  
SPECspeed®2017_fp_peak = 144

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You can also download the XML flags sources by saving the following links:

- [http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml](http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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