Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6146, 3.20GHz)

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</table>

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
  4.4.21-69-default
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.0 released May-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** jemalloc: jemalloc memory allocator library V5.0.1;
  jemalloc: configured and built at default for 32bit (i686) and 64bit (x86_64) targets
- **Power Management:** --

**Hardware**

- **CPU Name:** Intel Xeon Gold 6146
- **Max MHz:** 4200
- **Nominal:** 3200
- **Enabled:** 48 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 960 GB SSD SAS
- **Other:** None

**CPU2017 License:** 9019
**Test Sponsor:** Cisco Systems
**Test Date:** Oct-2017
**Hardware Availability:** Oct-2017
**Tested by:** Cisco Systems
**Software Availability:** Sep-2017
**SPECspeed®2017_int_base =** 9.88
**SPECspeed®2017_int_peak = Not Run**
SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6146, 3.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 9.88
SPECspeed®2017_int_peak = Not Run

Results Table

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.4, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Disabled
IMC Interleaving set to Auto

(Continued on next page)
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<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
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<tbody>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>Not Run</td>
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CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Oct-2017  
Hardware Availability: Oct-2017  
Software Availability: Sep-2017

Platform Notes (Continued)

Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f running on linux-g4f1 Tue Nov 14 10:48:36 2017

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
  4 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
  physical 0: cores 0 1 2 3 8 9 10 11 18 19 24 27
  physical 1: cores 0 1 2 3 4 9 10 16 18 19 25 26
  physical 2: cores 0 1 2 3 8 9 10 11 18 19 24 27
  physical 3: cores 0 1 2 3 4 8 10 11 18 24 25 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 12
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
Stepping: 4
CPU MHz: 1749.705
CPU max MHz: 4200.0000
CPU min MHz: 1200.0000
BogoMIPS: 6400.19
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-11

(Continued on next page)
Cisco Systems
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<table>
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## Platform Notes (Continued)

NUMA node1 CPU(s): 12-23
NUMA node2 CPU(s): 24-35
NUMA node3 CPU(s): 36-47

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpre pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_pkg_req intel_pt tpr_shadow vmx flexpriority ept vpid
fsgsbase tsc_adjust bml1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

/platforminfo cache data
  cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
  node 0 size: 192015 MB
  node 0 free: 190869 MB
  node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
  node 1 size: 193521 MB
  node 1 free: 192516 MB
  node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35
  node 2 size: 193521 MB
  node 2 free: 192458 MB
  node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47
  node 3 size: 193372 MB
  node 3 free: 190734 MB

node distances:
  node 0 1 2 3
  0: 10 21 21 21
  1: 21 10 21 21
  2: 21 21 10 21
  3: 21 21 21 10

From /proc/meminfo
  MemTotal:  790968596 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

/usr/bin/lsb_release -d
  SUSE Linux Enterprise Server 12 SP2

(Continued on next page)
**Platform Notes (Continued)**

From /etc/*release* /etc/*version*  
SuSE-release:  
    SUSE Linux Enterprise Server 12 (x86_64)  
    VERSION = 12  
    PATCHLEVEL = 2  
    # This file is deprecated and will be removed in a future service pack or release.  
    # Please check /etc/os-release for details about this release.  
    os-release:  
        NAME="SLES"  
        VERSION="12-SP2"  
        VERSION_ID="12.2"  
        PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"  
        ID="sles"  
        ANSI_COLOR="0;32"  
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:  
    Linux linux-g4f1 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)  
    x86_64 x86_64 x86_64 GNU/Linux  
    run-level 3 Nov 14 08:18 last=5  

SPEC is set to: /home/cpu2017  
    /dev/sda6      xfs   871G   77G  794G   9% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.  
    BIOS Cisco Systems, Inc. C480M5.3.1.0.248.0518171057 05/18/2017  
    Memory:  
        48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

**Compiler Version Notes**

```
C       | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)  
       | 625.x264_s(base) 657.xz_s(base)
```

icc (ICC) 18.0.0 20170811  
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

(Continued on next page)
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Compiler Version Notes (Continued)

C++
| 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
  |
| 641.leela_s(base)

icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Fortran | 648.exchange2_s(base)

ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
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Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

Base Other Flags

C benchmarks:
-m64 -std=c11

C++ benchmarks:
-m64

Fortran benchmarks:
-m64

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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