Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)  SPECspeed®2017 fp_base = 154
SPECspeed®2017 fp_peak = 155

| Software | SPECspeed®2017 fp_base = 154 | SPECspeed®2017 fp_peak = 155 |

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Nov-2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
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<td>Software Availability: Sep-2017</td>
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</table>

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017 fp_base</th>
<th>SPECspeed®2017 fp_peak</th>
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<tbody>
<tr>
<td>603.bwaves_s 48</td>
<td>203</td>
<td>154</td>
</tr>
<tr>
<td>607.cactuBSSN_s 48</td>
<td>205</td>
<td>155</td>
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<tr>
<td>619.lbm_s 48</td>
<td>80.3</td>
<td>54.7</td>
</tr>
<tr>
<td>621.wrf_s 48</td>
<td>85.2</td>
<td>59.0</td>
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<tr>
<td>627.cam4_s 48</td>
<td>116</td>
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<tr>
<td>628.pop2_s 48</td>
<td>116</td>
<td>88.6</td>
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<tr>
<td>638.imagick_s 48</td>
<td>121</td>
<td>116</td>
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<td>644.nab_s 48</td>
<td>305</td>
<td>122</td>
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<tr>
<td>649.fotonik3d_s 48</td>
<td>114</td>
<td>305</td>
</tr>
<tr>
<td>654.roms_s 48</td>
<td>223</td>
<td>230</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6146
- **Max MHz:** 4200
- **Nominal:** 3200
- **Enabled:** 48 cores, 4 chips
- **Orderable:** 2,4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Memroy:** 768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
- **Storage:** 1 x 600 GB SAS HDD, 10K RPM
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux;
  Fortran: Version 18.0.0.128 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.2.2a released Sep-2017
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **Power Management:** --
## SPEC CPU®2017 Floating Point Speed Result

### Cisco Systems

Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
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---

### Results Table

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<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>71.3</td>
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<td>220</td>
<td>70.5</td>
<td>223</td>
<td>70.0</td>
<td>225</td>
</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base = 154**  
**SPECspeed®2017_fp_peak = 155**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### General Notes

Environment variables set by runcpu before the start of the run:  
KMP_AFFINITY = "granularity=fine,compact"  
LD_LIBRARY_PATH = "/opt/cpu2017/lib/ia32:/opt/cpu2017/lib/intel64:/opt/cpu2017/je5.0.1-32:/opt/cpu2017/je5.0.1-64"  
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.4  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop_caches

---

### Platform Notes

BIOS Settings:  
Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS  
SNC set to Disabled  
IMC Interleaving set to Auto  
Patrol Scrub set to Disabled  
Sysinfo program /opt/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

SPEC CPU®2017 Floating Point Speed Result
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Platform Notes (Continued)

running on linux-vb5q Tue Jan 5 14:08:45 2010

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
 4 "physical id"s (chips)
 48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
physical 0: cores 0 3 4 5 6 7 16 18 19 20 21 22
physical 1: cores 0 3 4 5 6 7 16 18 19 20 21 22
physical 2: cores 0 1 3 9 10 16 18 19 24 25 26 27
physical 3: cores 0 1 3 9 10 16 18 19 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: LittleEndian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 12
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
Stepping: 4
CPU MHz: 1200.176
CPU max MHz: 4200.0000
CPU min MHz: 1200.0000
BogoMIPS: 6400.04
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-11
NUMA node1 CPU(s): 12-23
NUMA node2 CPU(s): 24-35
NUMA node3 CPU(s): 36-47

(Continued on next page)
Cisco Systems
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Platform Notes (Continued)

Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3nowprefetch ida arat epb pln pts dtherm hwp
hwp_act_window hwp_epp hwp_kpg_req intel_pt tpr_shadow vmmi flexpriority ept vpid
fsgsbase tsc_adjust cpl hle avx2 smep bmi2 erna invpcid rtm cqm mpx avx512f
avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsavec
xgetbv1 cqm_llc cqm_occup_llc

/platform/cpuinfo cache data
  cache size : 25344 KB

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
  node 0 size: 191928 MB
  node 0 free: 186913 MB
  node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
  node 1 size: 193521 MB
  node 1 free: 192151 MB
  node 2 cpus: 24 25 26 27 28 29 30 31 32 33 34 35
  node 2 size: 193521 MB
  node 2 free: 192148 MB
  node 3 cpus: 36 37 38 39 40 41 42 43 44 45 46 47
  node 3 size: 193518 MB
  node 3 free: 192408 MB
  node distances:
    node  0   1   2   3
    0:  10  21  21  21
    1:  21  10  21  21
    2:  21  21  10  21
    3:  21  21  21  10

From /proc/meminfo
  MemTotal:       791029124 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.

(Continued on next page)
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Platform Notes (Continued)

# Please check /etc/os-release for details about this release.
os-release:
  NAME="SLES"
  VERSION="12-SP2"
  VERSION_ID="12.2"
  PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
  ID="sles"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
  Linux linux-vb5q 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016 (9464f67)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Jan 4 23:04

SPEC is set to: /opt/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda1 xfs 280G 108G 172G 39% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017
  Memory:
    48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C                | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
| 644.nab_s(base, peak)
==============================================================================
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
==============================================================================

C++, C, Fortran    | 607.cactuBSSN_s(base, peak)
==============================================================================
icpc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811

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Compiler Version Notes (Continued)

Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

==============================================================================
Fortran, C | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
==============================================================================
ifort (IFORT) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.
icc (ICC) 18.0.0 20170811
Copyright (C) 1985-2017 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian

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Base Portability Flags (Continued)

627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Base Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11
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---

Peak Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

---

Peak Portability Flags

Same as Base Portability Flags

---

Peak Optimization Flags

C benchmarks:

619.lbm_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP

638.imagick_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP

644.nab_s: Same as 638.imagick_s

Fortran benchmarks:

-no-prec-div -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3 -qopenmp

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=3 -DSPEC_SUPPRESS_OPENMP -qopenmp

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Peak Optimization Flags (Continued)

621.wrf_s (continued):
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

627.cam4.s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs -align array32byte

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-prefetch
-ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs
-align array32byte

Peak Other Flags

C benchmarks:
-m64 -std=c11

Fortran benchmarks:
-m64

Benchmarks using both Fortran and C:
-m64 -std=c11

Benchmarks using Fortran, C, and C++:
-m64 -std=c11

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic18.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2010-01-05 14:08:44-0500.
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